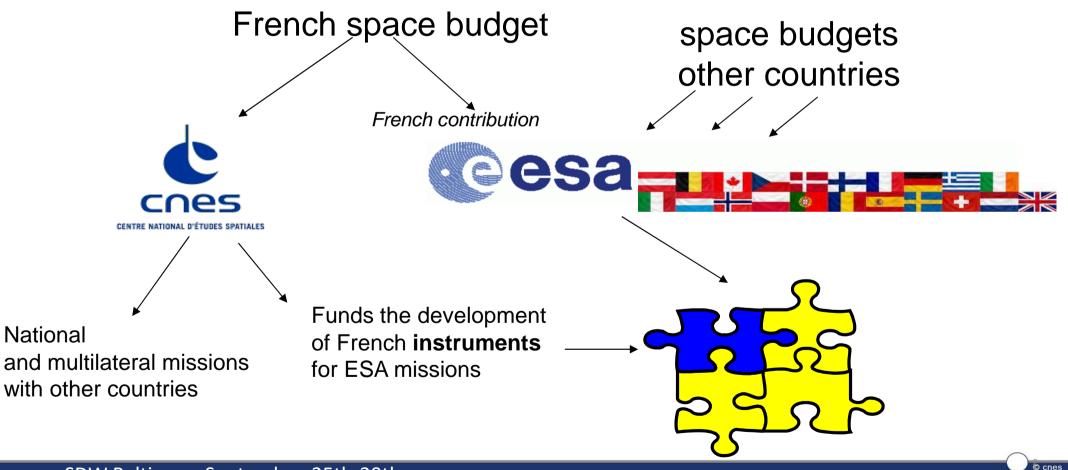
CNES detector development for scientific space missions: status and roadmap for infrared detectors

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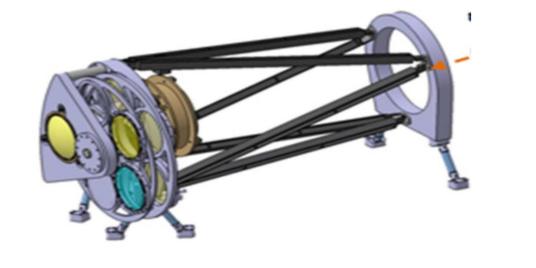


Euclid

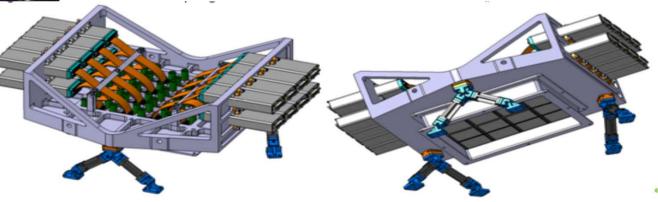


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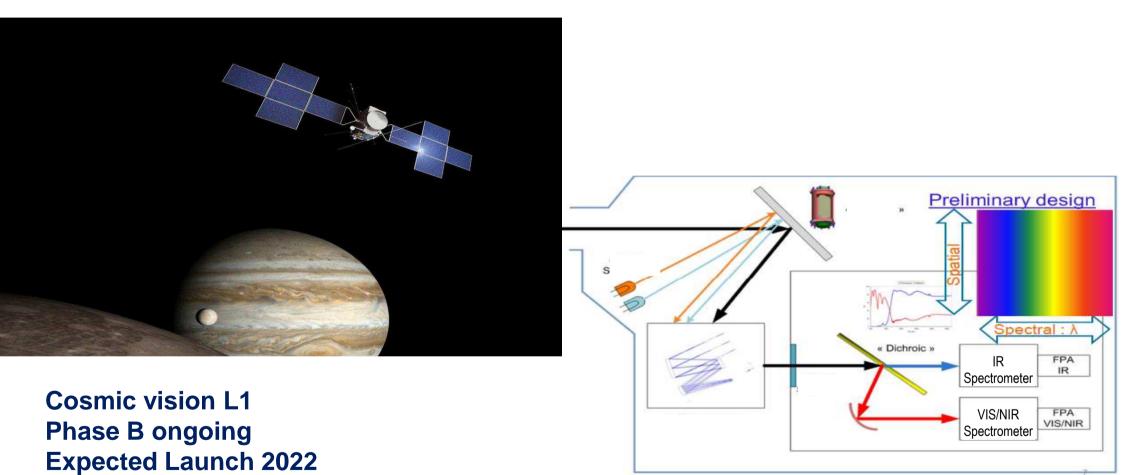


Cosmic vision M2 CDR passed Expected Launch 2020



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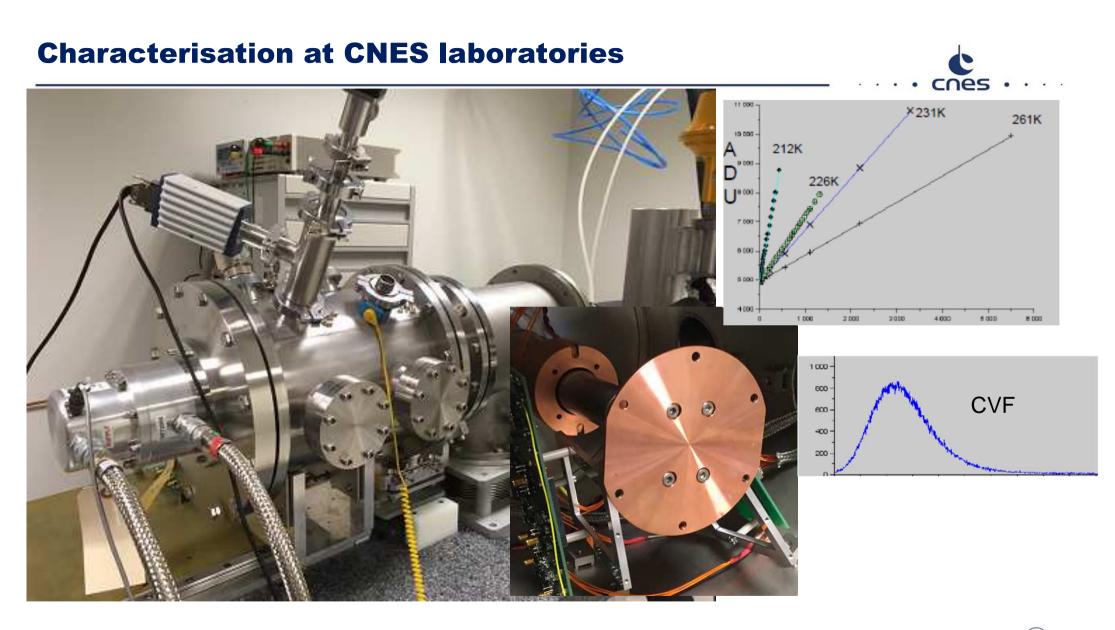






Cosmic vision : M4 candidate currently in phase A Expected Launch 2026

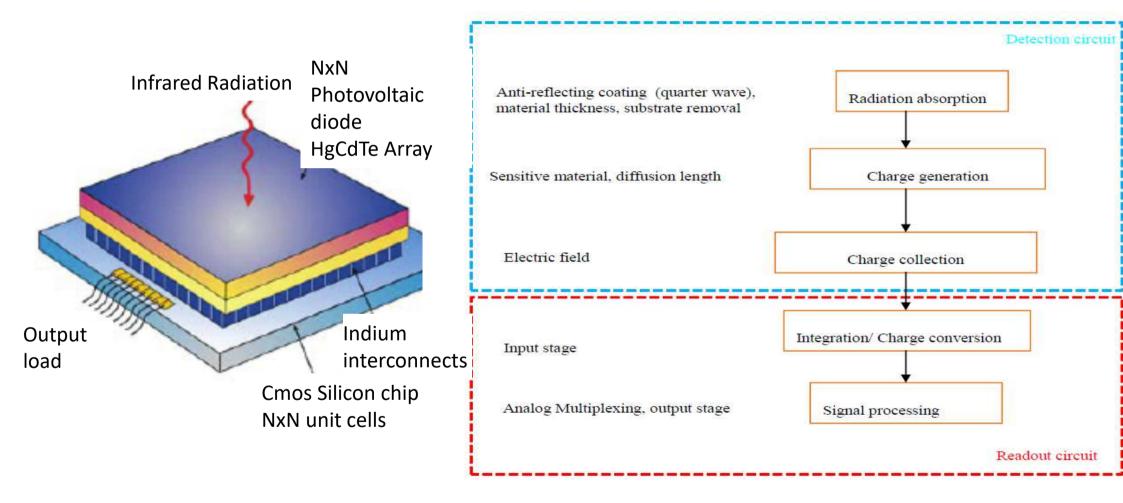
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The HgCdTe Infrared Detector





Key technologies of HgCdTe infrared detectors for scientific ap<u>plication</u>

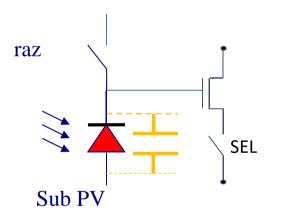
- Large format detectors from 1k² to 2k² arrays : need to overcome strong technological limitations
- Low readout noise detectors
- A specific input stage for very low flux : SFD (Source Follower per detector) : Very low flux, very low power, low noise, glow free
- Another solution : APD (Avalanche Photodiode) technology: allows a signal gain at diode level (demonstrated for n/p diode)
- Photodiode p/n technology: is necessary to achieve low dark current and allows good signal to noise ratio performance

CNES developments to prepare future space missions

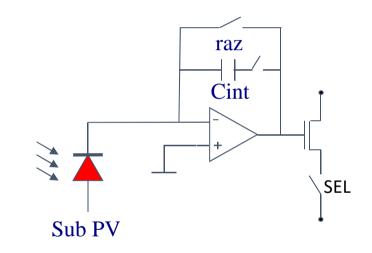
ReadOut Circuit (ROIC) input stages



SFD (Source Follower Detector) Integration on detector node



CTIA (Capacitive Transimpedance Amplifier)



ReadOut Circuits (ROIC) input stages



Performance	SFD	CTIA	Comments
Noise without CDS	15-20e- rms typ.	30-150 é rms (lower limit)	The noise figure can be lowered with CDS or multiple (and non- destructive) readout. Few e- rms noise can be reached with SFD
Flux range	0.01 e-/s/pixel to <10 ⁴ e-/s/pixel	few 10 ⁴ e-/s/pixel to few 10 ⁸ e-/s/pixel typ.	
Charge capacity	< 10 ⁵ e- typ.	10 ⁵ e- to few 10 ⁶ e- typ.	Charge capacity depends on the photodiode wavelength detection range for SFD
Readout frequency	up to 500 kHz	up to 20 MHz	SFD ROIC drive an output capacitance of ~few pF, whereas CTIA ROIC can drive ~100 pF capacitance
Power dissipation	1 mW typ.	50-150mW	

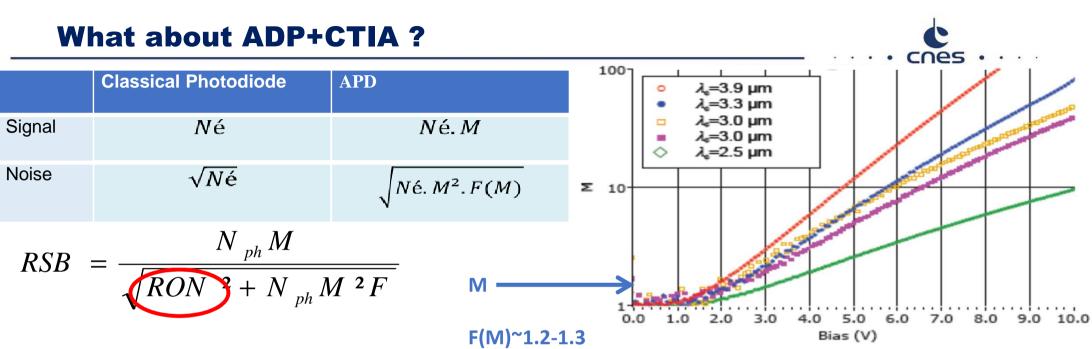


Main intrinsic limitation of the SFD input stage :

- Relatively small integration capacity (associated with a large potential offset dispersion) which limits its use for "medium input fluxes".
- Low frequency readout/poor capability to drive large impedance (needs for intermediate electronics stage at low temperature)
- Electronics operating point to be tune finely

Main limitation of the CTIA input stage :

- Compatibility with input fluxes in the range few 10² to 10³ e-/s/pixel?
- Glow (self-parasitic light) effect from the ROIC itself and/or current leakage effects can affect the performance, either by degrading the noise budget (parasitic flux), or the linearity at very low level (floor/threshold effect,...).

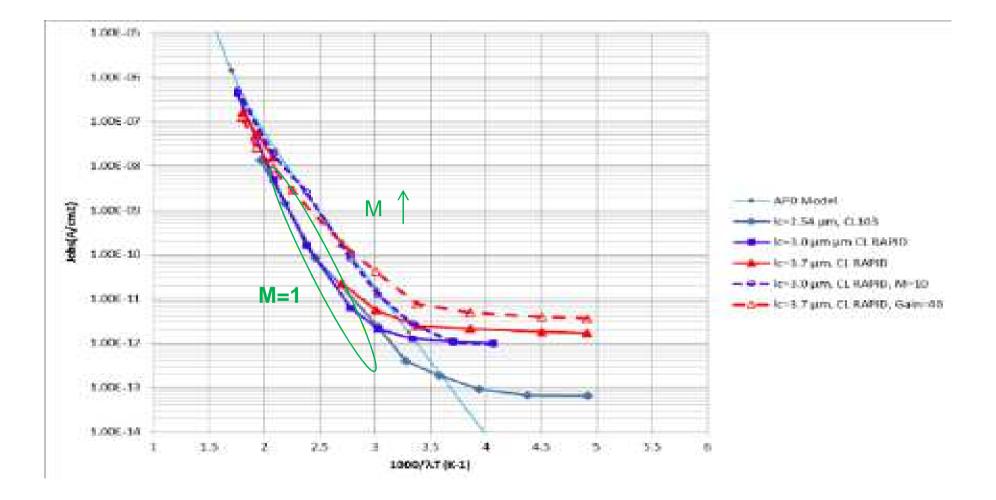


Still open points to be addressed in order to reach a good performance:

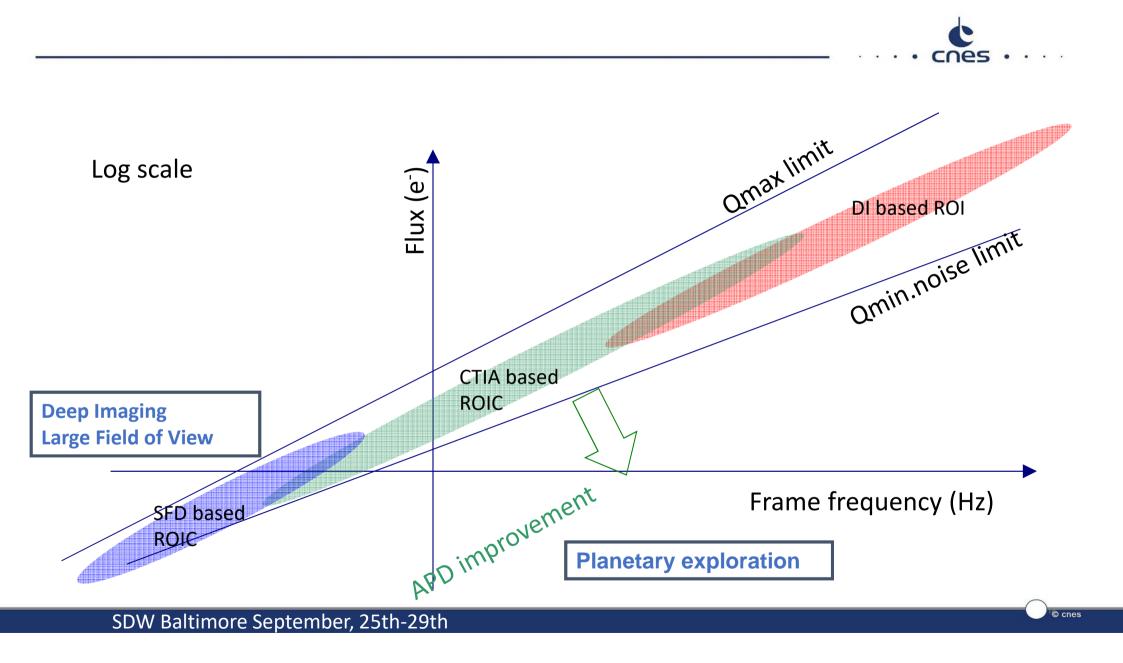
- CTIA parasitic current of the order of 50-100 electron/s: too high wrt requirements (~< 1 electron/s)
- n/p APDs are difficult to use for cutoff wavelength below ~3µm
 - the smaller is the wavelength the higher is the bias needed
- dark current signal levels are still higher than the requirement (G-R dark currents)

Dark current contribution in APD



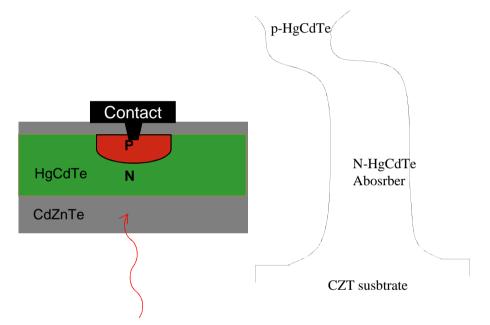


Cnes



p/n photodiode technology





Dark signal < 0.1é/s needs:

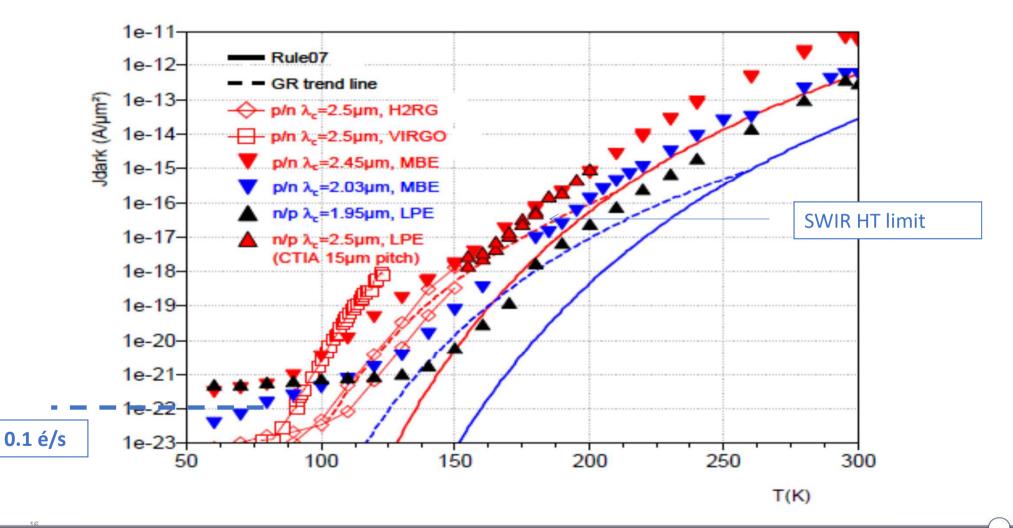
- High quality HgCdTe material
- Optimized junction process
 - Graded junction
 - control of the doping level



- CNES developments :
 - NIR/SWIR bands (cutoff wavelength > 2µm@77K), LPE process
 - Joint effort with Earth observation mission (FPA temperature < 150K)
 - LWIR bands (cutoff wavelength ~12 µm@40K), LPE process
 - Echo mission

SWIR p/n results

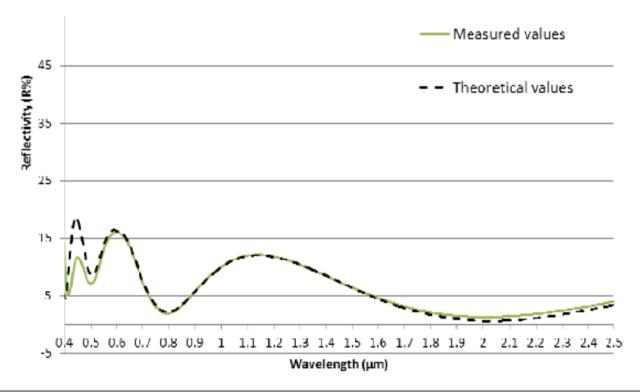




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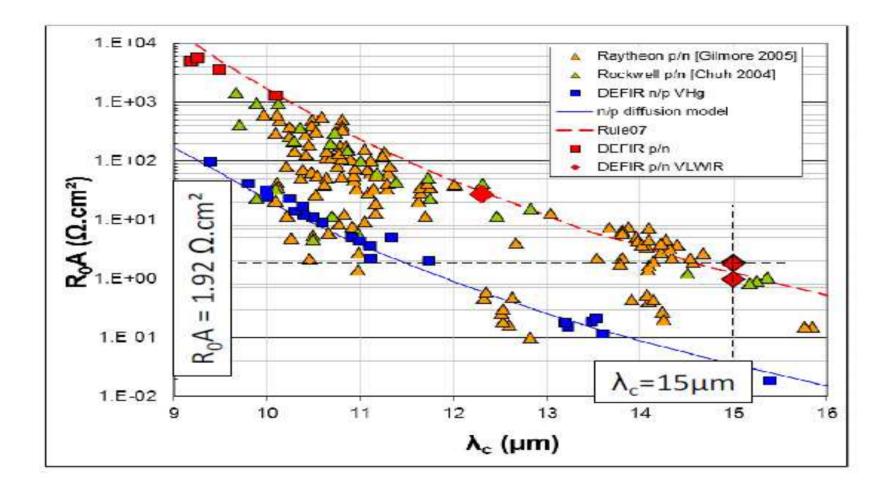


- Increase of the sensitivity on a large spectral band
- ARC deposition should not impact detector performances: processes and handling are critical



LWIR p/n results





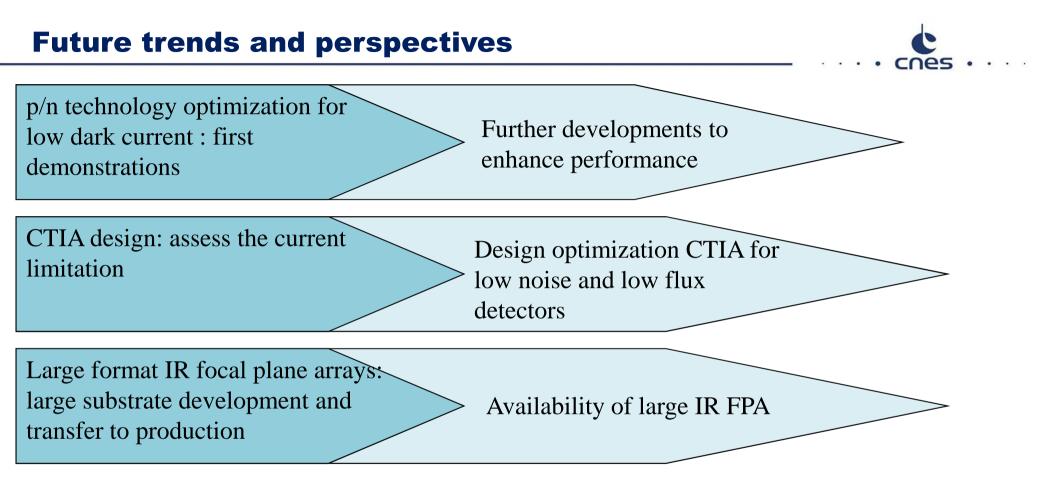
Large Format Infrared Detector Arrays



- Main challenges are:
 - Stitching capability of the CMOS foundry
 - Large substrate growth
 - Hybridization technology



- Current developments are focusing on two main topics:
- Enhancement of the production capabilities for array format of 1kx1k pixels or more
- Large detection circuits fabrication: Sofradir and CEA-LETI have shown excellent control of CZT ingots fabrication:
 - 3.5" CZT substrate size is now under production
 - HgCdTe epilayer deposition is well-controlled and within the production standard
 - Photodiode processes on large substrates has been demonstrated.



- ESA is currently developing a 2K² SWIR based on SFD ROIC and p/n technology
- Coordination and joint efforts with ESA and French Laboratories (Labex Focus) for those developments



Acknowledgements

To ESA and Labex Focus for their partnership

To the teams who have worked on those developments (CEA-LETI, CEA-Irfu, Sofradir)

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