Developments in CCD and CMOS Detectors at MIT Lincoln Laboratory

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Scientific Detector Workshop
7 October 2013

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

MIT Lincoln Laboratory

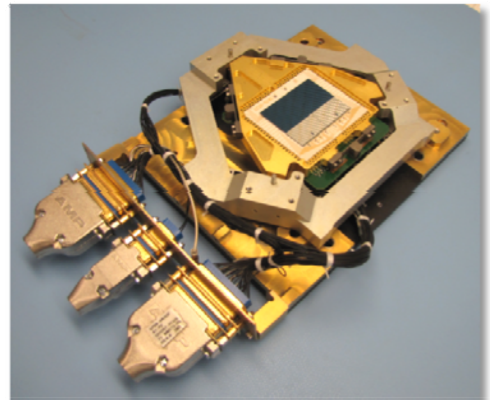
- **Federally-Funded Research and Development Center (FFRDC) run by the Massachusetts Institute of Technology under contract with the Air Force. Located on Hanscom Air Force Base in Lexington, MA**
  - **~3800 employees**
  - **~$940M/yr (FY12) sponsored research**

- **Primary focus is on the development of prototype radar, communications, and surveillance systems for the DoD and other government agencies**
  - **Conduct research in advanced electronics technology to support and enable new prototype system development**
  - **Growing segment in industrial-sponsored research through CRDA**
- **Work with US industry to transfer Lincoln Laboratory technology to meet future DoD and government needs**

Unique Focal-Plane Technology in Support of National Security

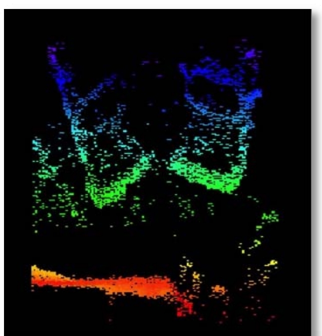
Space Surveillance

AMOS (AF)



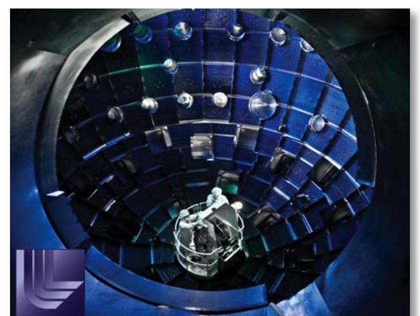
DoD Satellites

Directed Energy AFRL SOR



Laser Radar

Astronomy

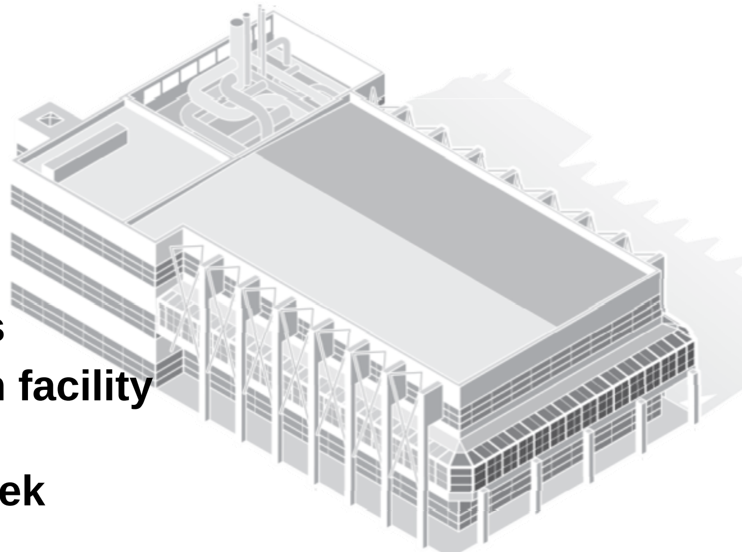


National Ignition Facility (LLNL)

Nuclear Stockpile Stewardship (LANL)

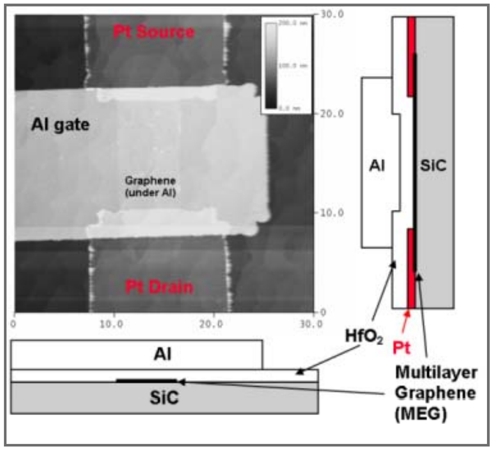
Microelectronics Laboratory

- **Specially designed 70,000 square foot building**
  - First completed silicon (Spring 1993)
  - Converted to 150 mm wafer processing in 1996
  - Converted to 200 mm wafer processing (Spring 2011)
- **Clean Room space**
  - 8,100 Square feet of class-10
  - 10,000 Square feet of class-100
- **Microelectronics Laboratory activities**
  - > 30 Active programs in support of 4 divisions
  - > 65 People from 5 groups working full-time in facility (Scientists, Engineers, and Technicians)
  - Two-shift operation, 6 am to 11 pm, 5 days/week

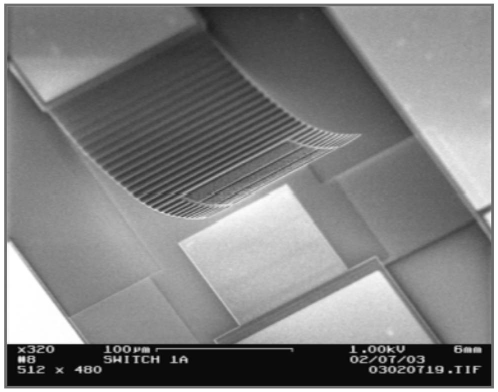


Facility/Equipment Value ~$175-200M

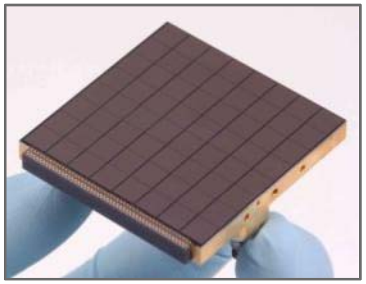
Spanning Research to Low-Volume Prototyping in One Facility

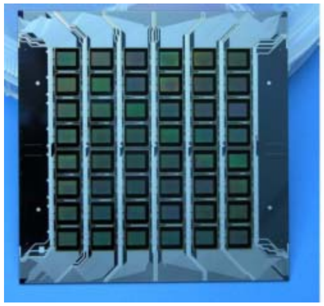


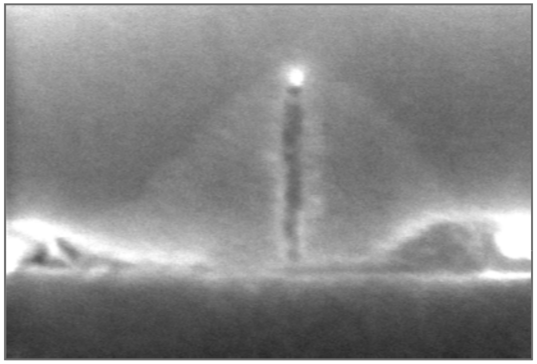
Graphene Devices

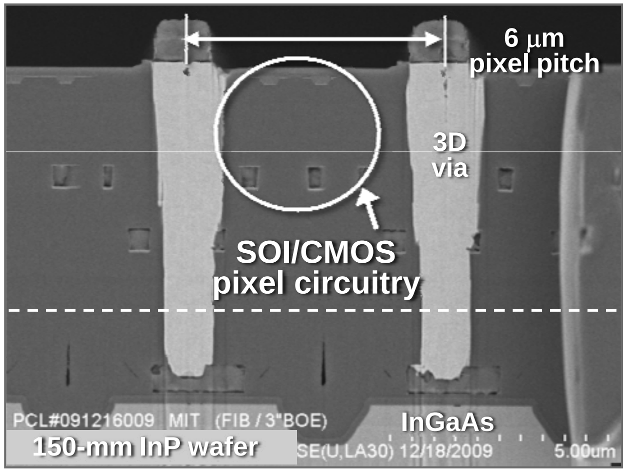


MEMS RF Switches

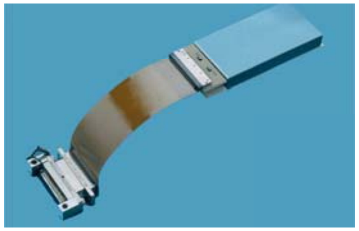

22M-pixel Orthogonal Transfer Array Focal Plane Tiles


MASIVS Focal Plane Array


9-nm Gate-Length Fully Depleted SOI

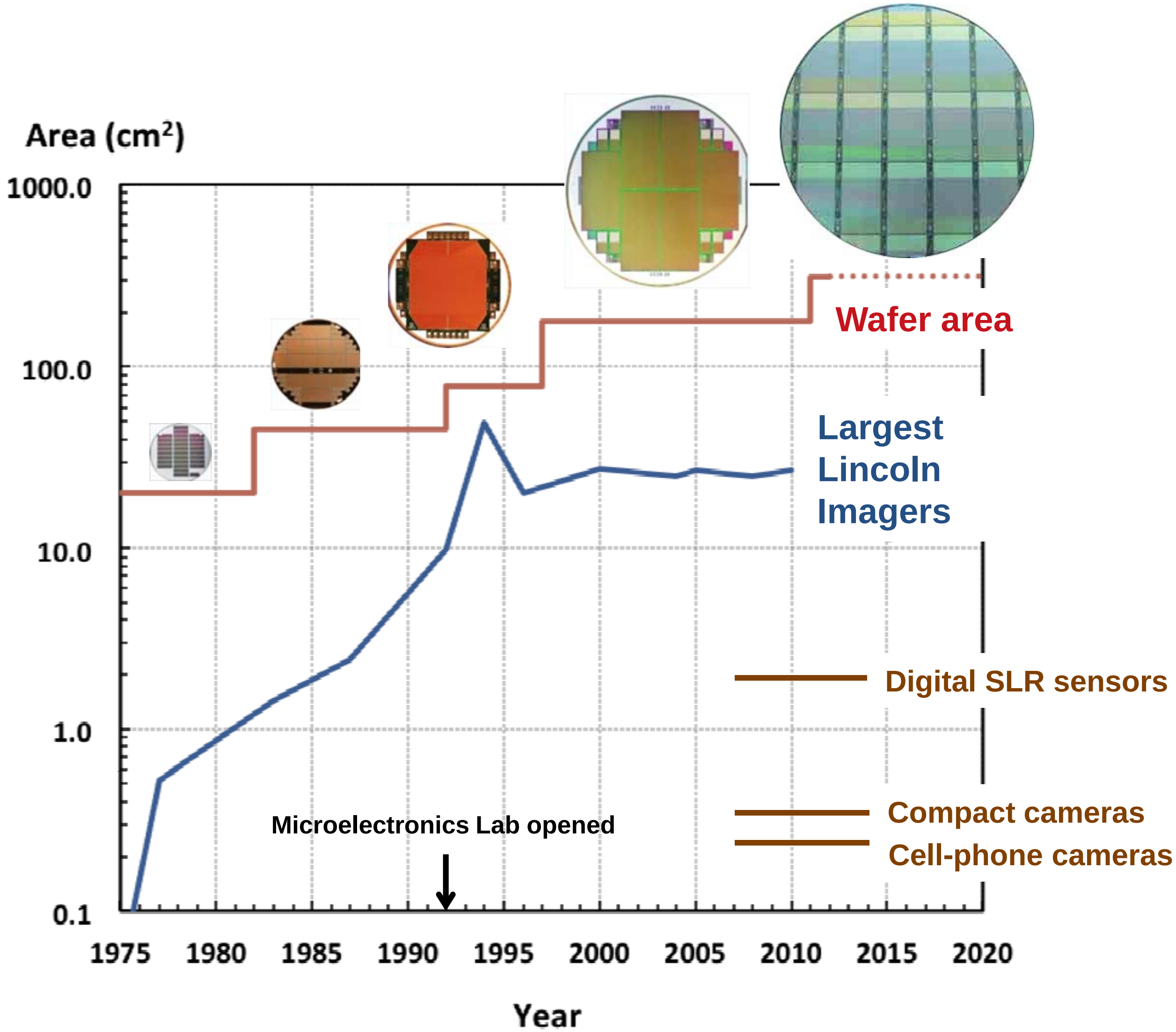


InP/CMOS 3-D Integration of SWIR FPA


Curved CCD Focal Plane Arrays for Space Surveillance Telescope

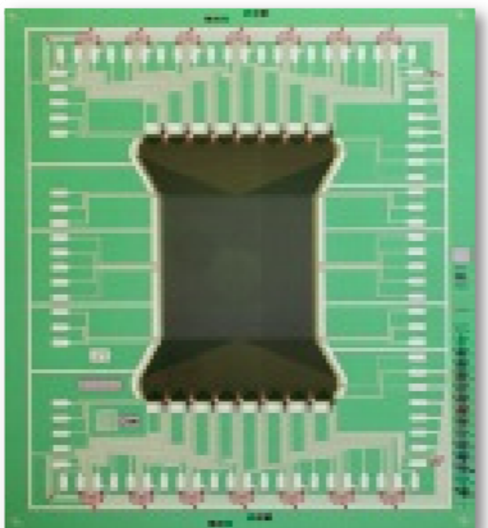
Device Research/ Novel Materials → **Demonstration Circuits/Devices** → **Low volume, specialized, sophisticated prototypes**

Growth in Wafer and Device Sizes

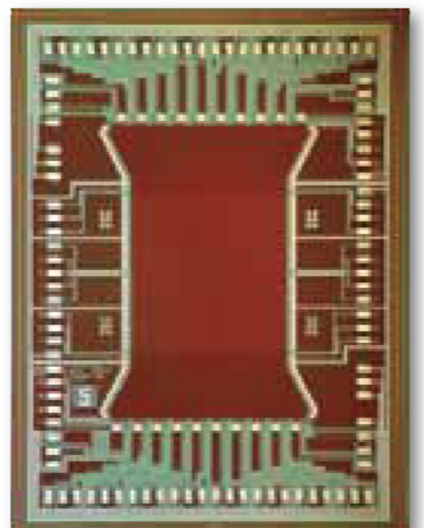


Existing Sensors for Adaptive Optics

Device	Format (Ports)	Pixel Size	Frame Rate	Read Noise	Comment
CCID26	**128 × 128 (16)**	**21 µm**	**2.5 kfps**	**7 e^-**	**Electronic shutter**
CCID66	**160 × 160 (20)**	**21 µm**	**2.5 kfps**	**4 e^-**	**High-responsivity pJFET charge-sense with two-stage on-chip amplification**

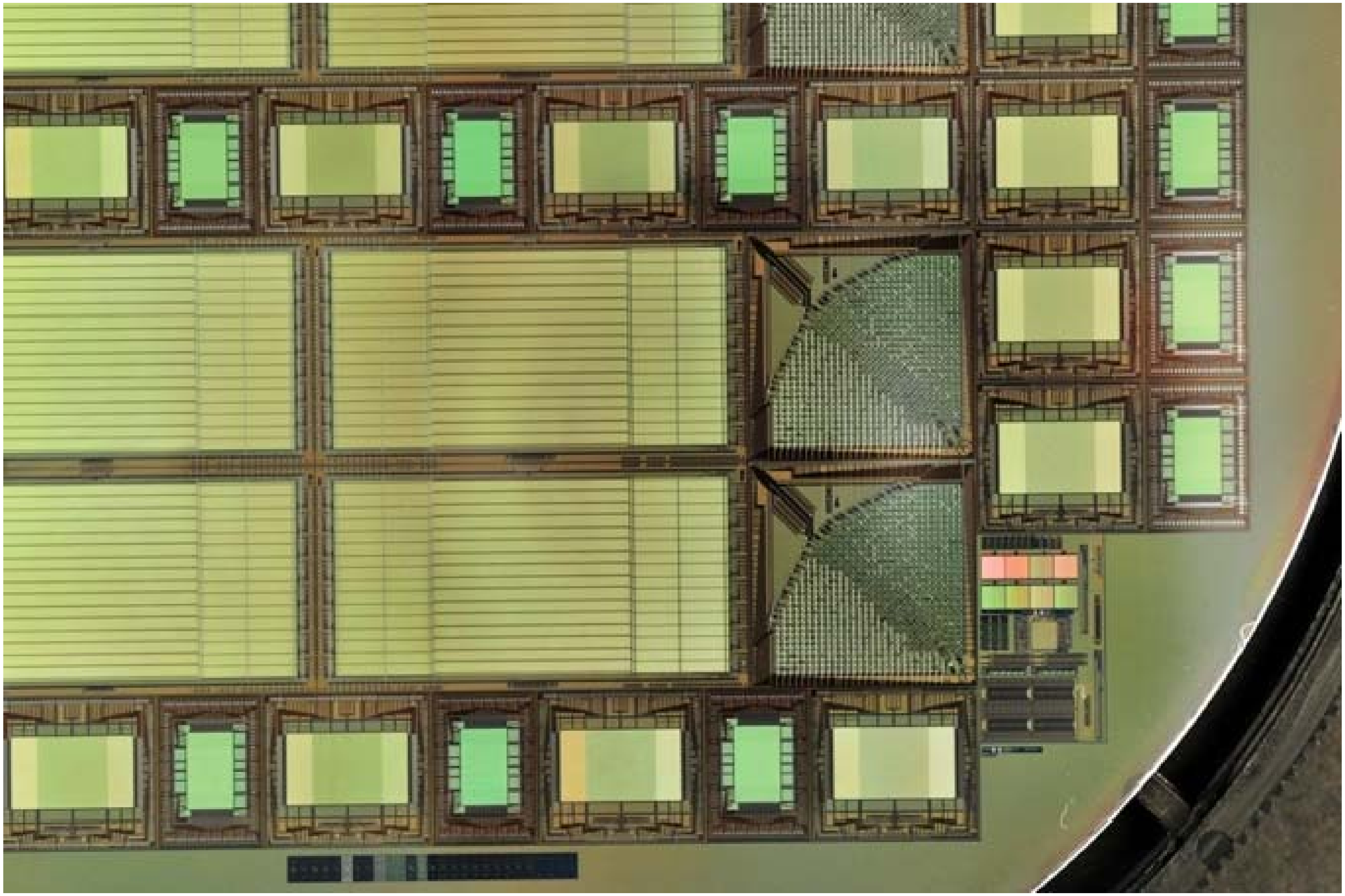


Die Photo MITLL CCID26



Die Photo MITLL CCID66

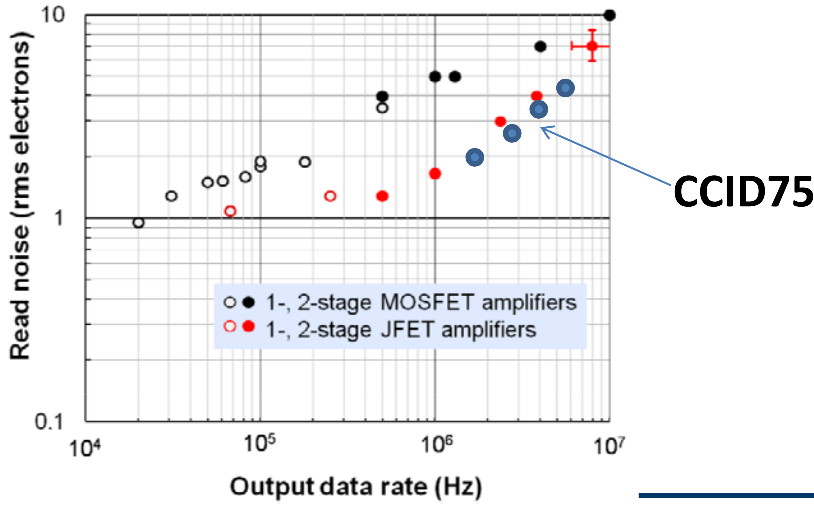
Photomicrograph Detail of Wafer



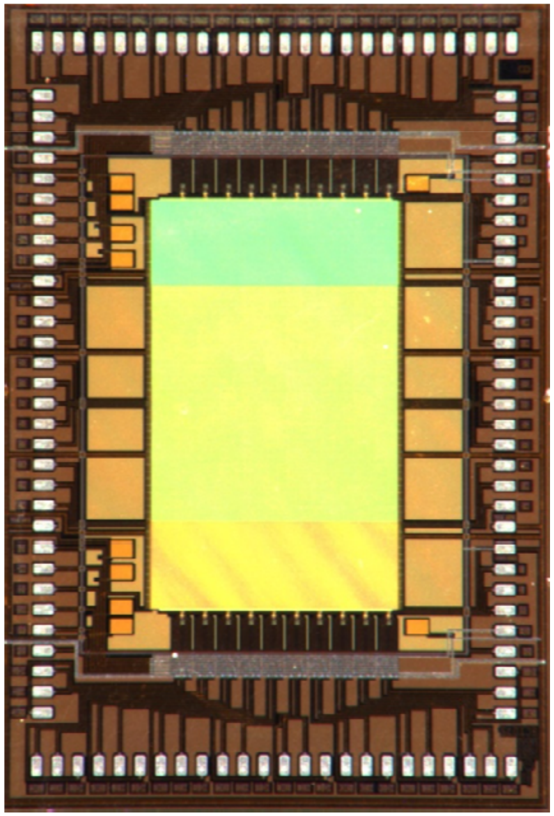
Evolutionary Technology Enhance NIR Sensitive AO CCD

- **MIT-LL CCID75: Adaptive Optics CCD with readout port isolation and region-of-interest for high-frame-rate / low-latency operation**

Design Parameter	Goal
Array Size	**160 × 160**
Pixel Pitch	**21 µm**
Well Depth	**> 50,000 e⁻**
Wavelength	**0.4 – 1.1 µm**
Frame Rate	**2.5 kfps**



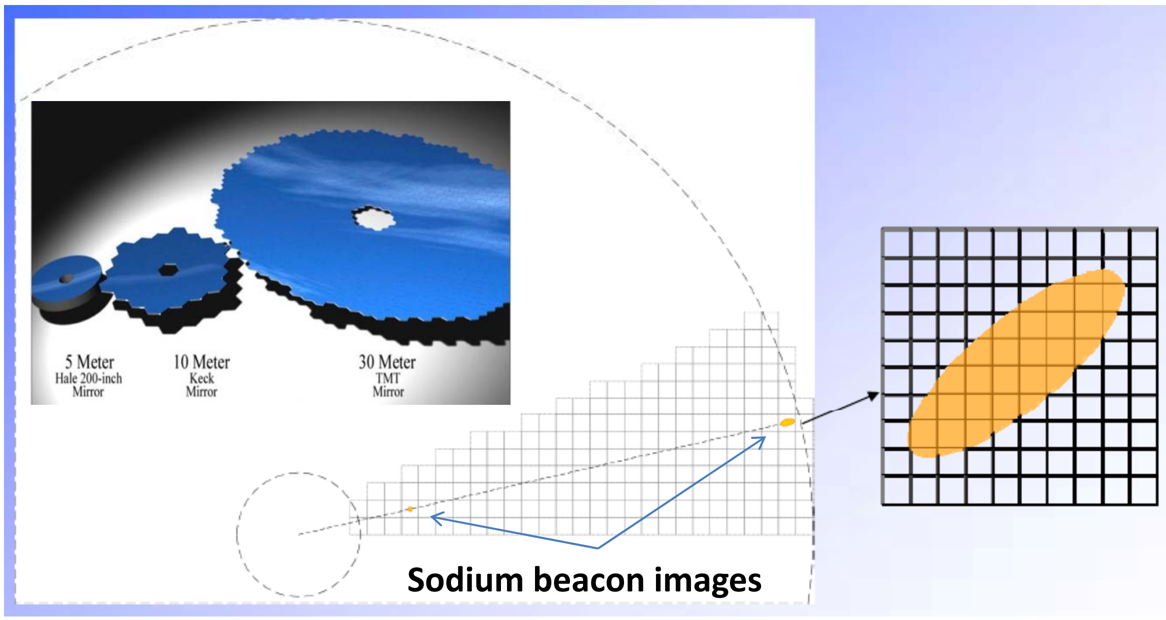
CCID75 Photograph

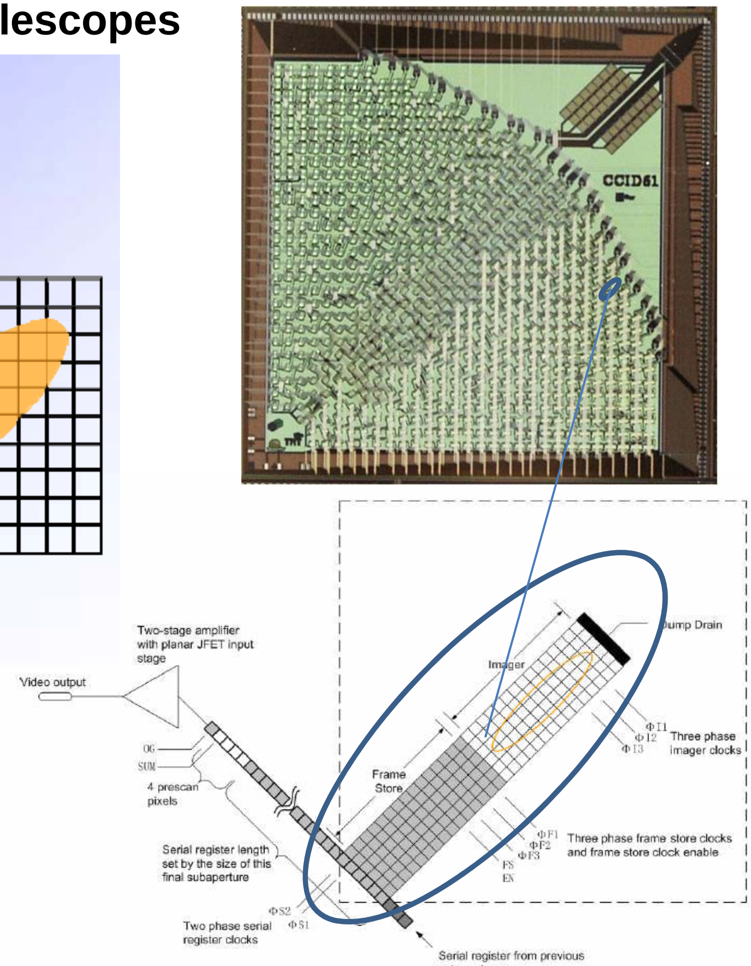


Targeted Technology
Polar Coordinate Imager

Sensors for Adaptive Optics

- **Example: Polar coordinate imaging to address the challenge of Adaptive Optics for extremely-large telescopes**





- **Sodium beacon image elongates radially as the distance from center of the focal plane increase**
- **Many small CCD arrays located and oriented to optimally sample each sub-aperature**

Front illumination test results

Courtesy S. M. Adkins
W. M. KECK OBSERVATORY

Device	L1-W1-C3	L1-W3-C1	Units
Read noise	3.47	3.24	e-
Full well	26844	24967	e-
Non-linearity	1.2	1.4	%
Responsivity	15	16	µV/e-
Dark current	~10*	~2.1	e-/pixel/s
Serial CTE	0.999991	0.999993	-
Parallel CTE	0.999990	0.999990	-
Charge diffusion	0.25	0.37	pixels

** = device operated at -8 °C*

- **L1-W1-C3 was not baked and has an epoxy seal**
- **Later determined devices were operating at ~ -15 C and ~ -29 C**

Read noise, gain, full well

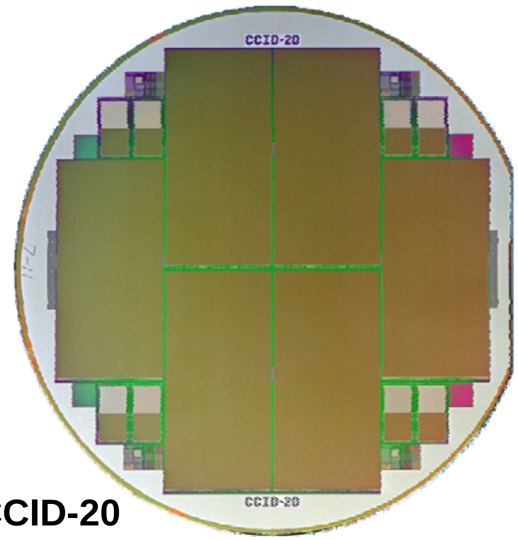
Courtesy S. M. Adkins

W. M. KECK OBSERVATORY

Device	L1-W1-C3																
Video channel	**Average**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
Read noise	3.46	3.71	3.73	3.23	2.96	3.61	3.26	3.28	3.71	3.70	3.54	3.69	3.45	3.54	3.28	3.32	3.35
Gain (e-/DN)	0.53	0.56	0.56	0.50	0.48	0.52	0.52	0.55	0.53	0.55	0.54	0.56	0.54	0.53	0.49	0.53	0.56
Full well	26714	26806	25122	25305	27528	25095	24579	28898	26129	29114	27378	26000	27847	26691	26558	26989	27377
Video channel	**Average**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**
Read noise	3.48	3.15	3.60	3.10	3.74	3.63	3.12	3.63	3.79	3.74	3.70	3.74	3.42	3.11	3.19	3.75	3.28
Gain (e-/DN)	0.54	0.50	0.55	0.53	0.52	0.53	0.54	0.55	0.54	0.54	0.50	0.53	0.55	0.55	0.56	0.54	0.56
Full well	26974	26945	27507	28402	24927	27365	28108	27896	28758	27847	26008	25474	26388	27306	24502	28523	25624

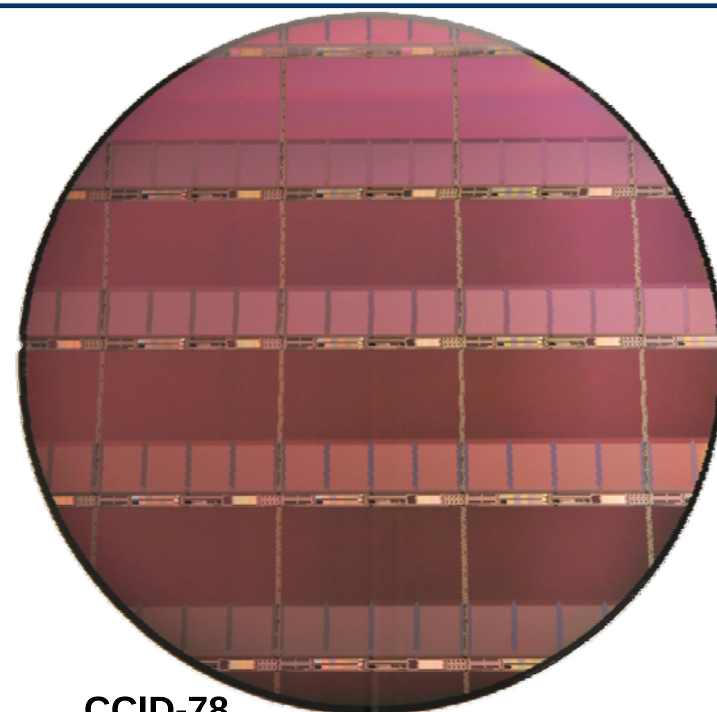
Device	L1-W3-C1																
Video channel	**Average**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
Read noise	3.18	3.20	2.83	3.63	3.28	3.54	3.24	3.68	2.84	3.01	2.89	3.15	3.66	2.77	3.04	3.25	2.77
Gain (e-/DN)	0.52	0.46	0.50	0.51	0.50	0.51	0.49	0.49	0.45	0.54	0.52	0.56	0.57	0.54	0.57	0.54	0.55
Full well	25452	24590	26281	26004	23839	24258	26982	24813	24676	23702	26312	24779	26802	25365	27091	24873	26864
Video channel	**Average**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**
Read noise	3.30	3.57	3.65	2.86	3.75	2.95	2.86	3.49	3.04	3.13	3.71	2.87	3.50	2.95	3.66	3.19	3.64
Gain (e-/DN)	0.52	0.53	0.50	0.57	0.47	0.53	0.50	0.54	0.45	0.55	0.53	0.56	0.56	0.52	0.51	0.50	0.50
Full well	24482	23327	25106	22943	23667	23141	24771	23276	26526	25514	26141	25086	25412	24347	25053	23157	24247

Transition from 150-mm to 200-mm Wafers



CCID-20

150 mm



CCID-78

200 mm

SVG i-line Scanner

1× scanner (150-mm field)

~500 nm overlay typ.

2-µm resolution typ.

Canon i-line Stepper (0.25 NA)

< 100-nm overlay

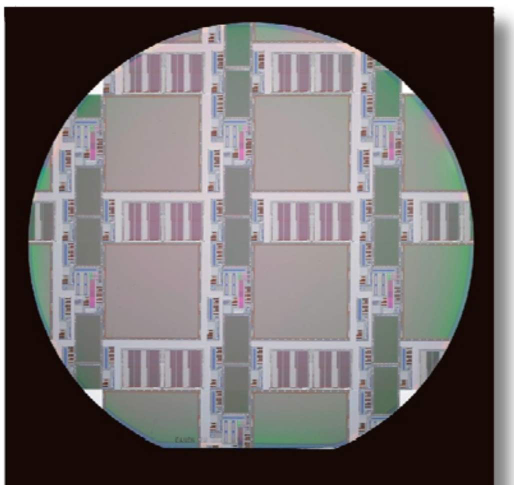
800-nm resolution

2× stepper (> 50 × 50 mm field)

I-line Stepper Lithography 200-mm Wafer Capability Demonstrators

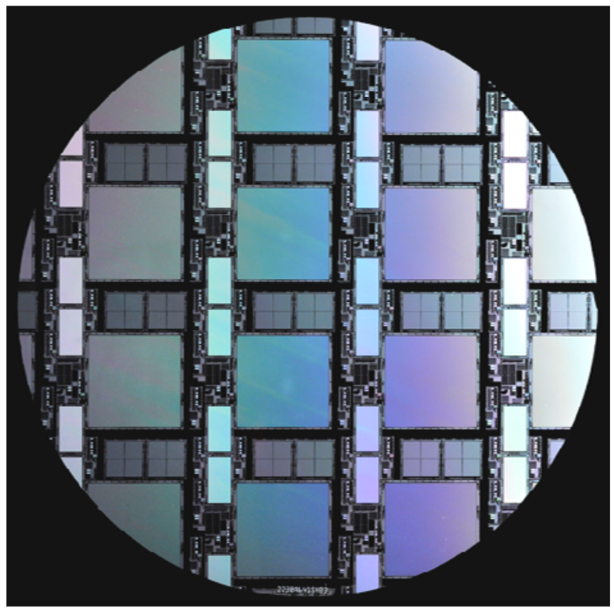
Same Reticle Used

Full Field Stepping



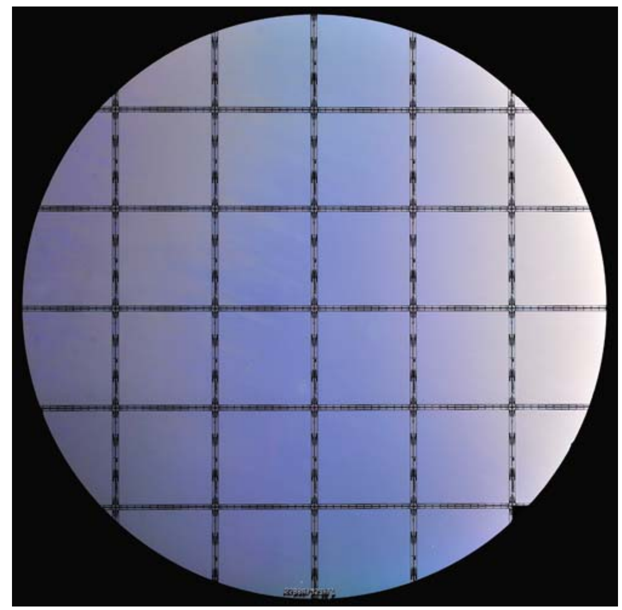
150 mm

Full Field Stepping



200 mm

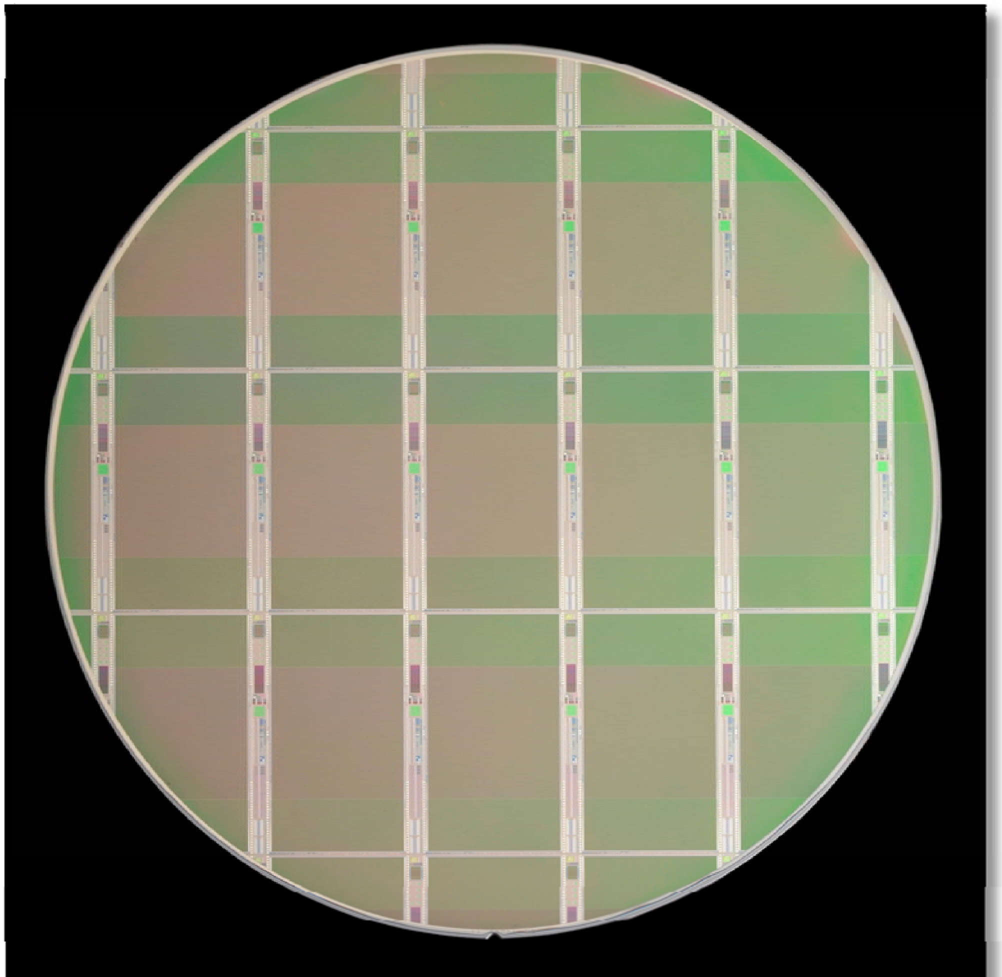
16 CCDs Per Wafer

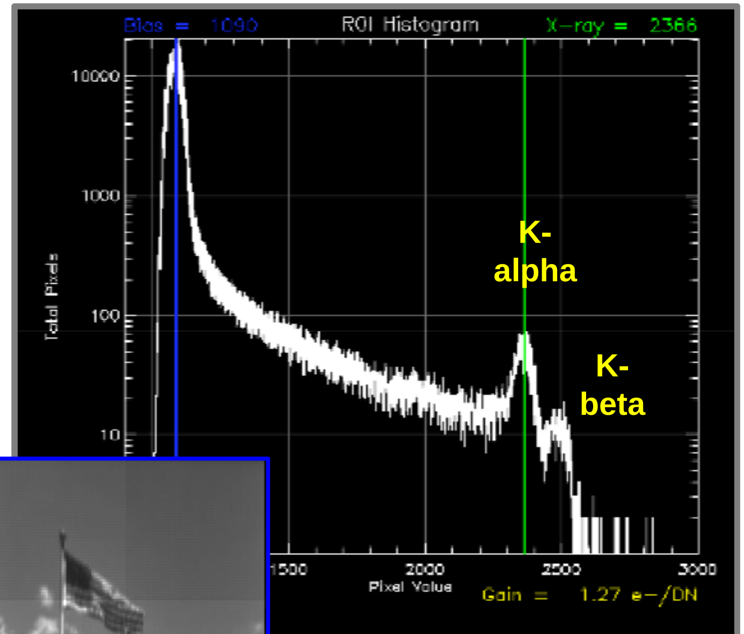


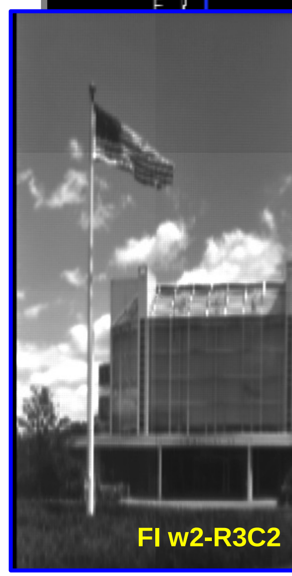
200 mm

FI = Front Illuminated

Results from First 200-mm CCD Lot
3k x 3k Image Array and Frame Store (9.5µm pixel)

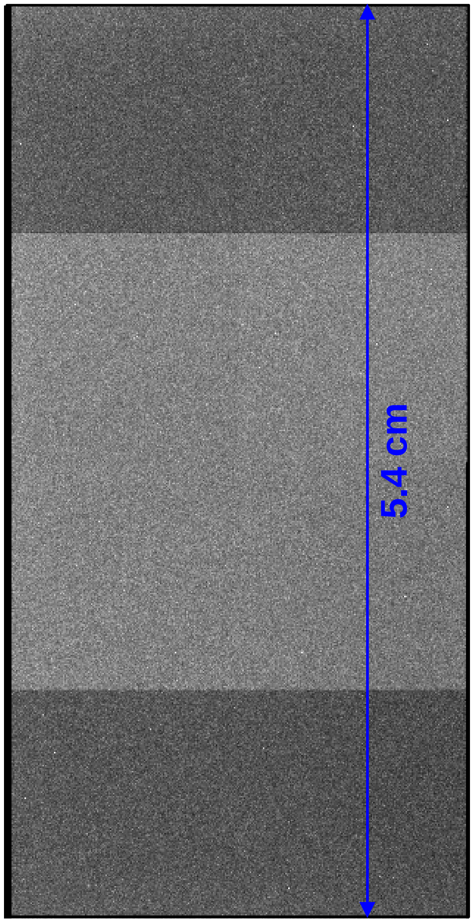






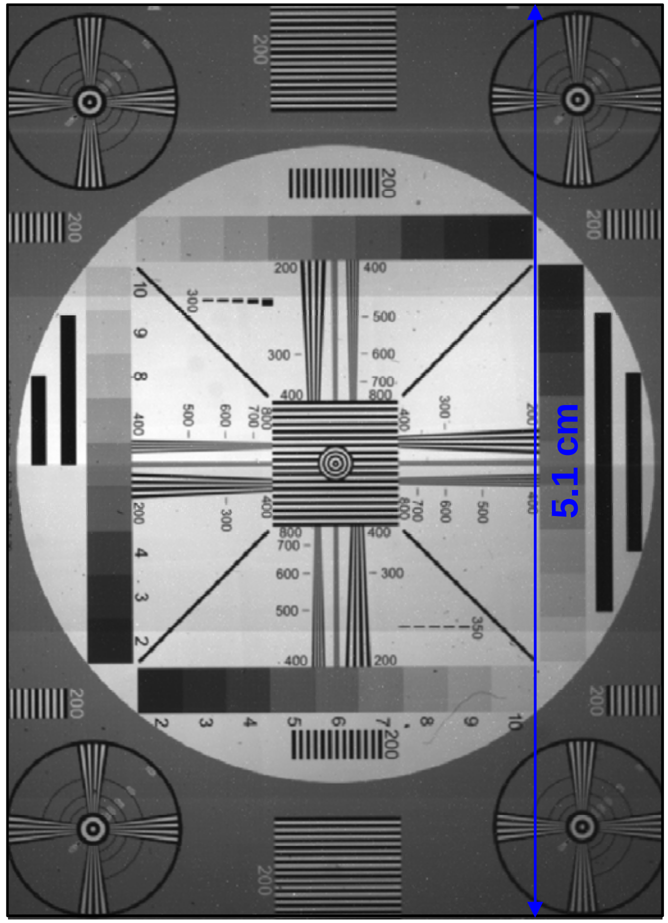
Uniformity of Large Area CCDs

FI 3k x 3k



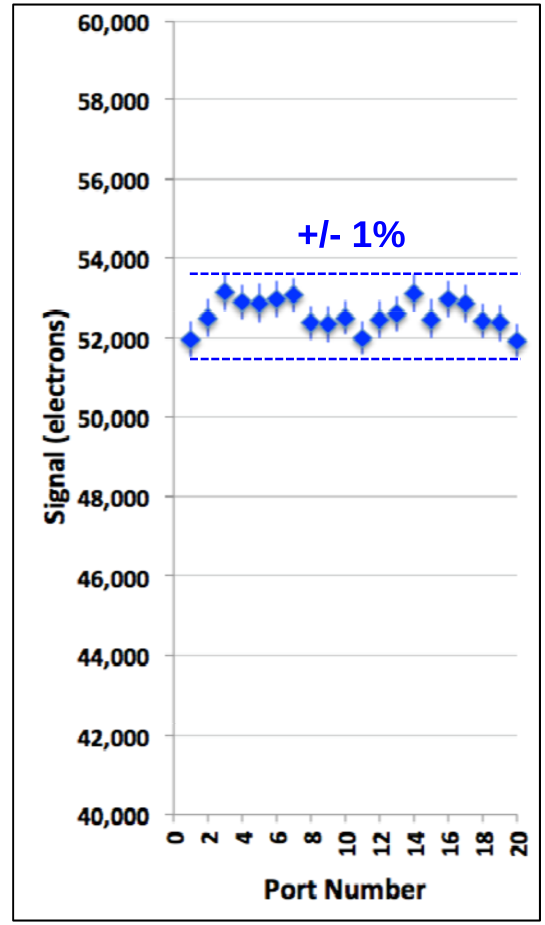
60 sec integration at -20°C

BI 1k x 2k



BICCID-78 L1a-W1-C7 Imaging Array at -30°C using 430 nm LED

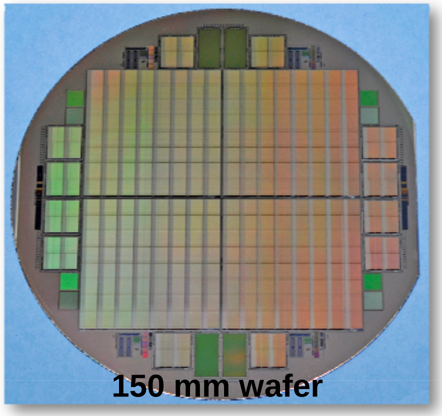
Output Circuits

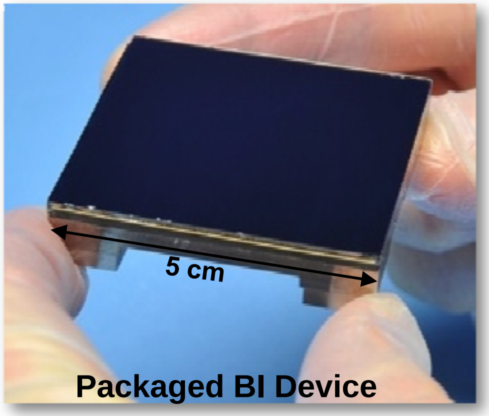


20-port Adaptive Optics Device CCID75

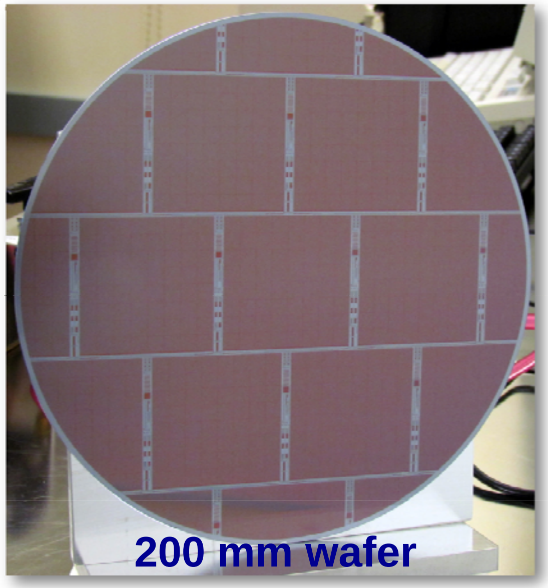
Orthogonal Transfer Arrays for Pan-STARRS GPC2

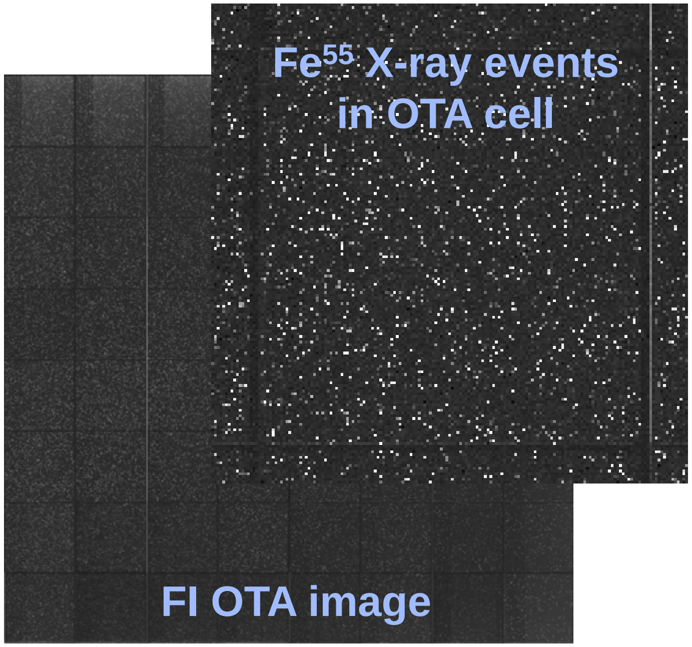
- **Device Improvements (CCID71)**
  - Improved video quality by using only 2-phase devices
  - Increased full well
  - Improved fill factor
  - Reduced persistence and amplifier glow
  - Better AR coating





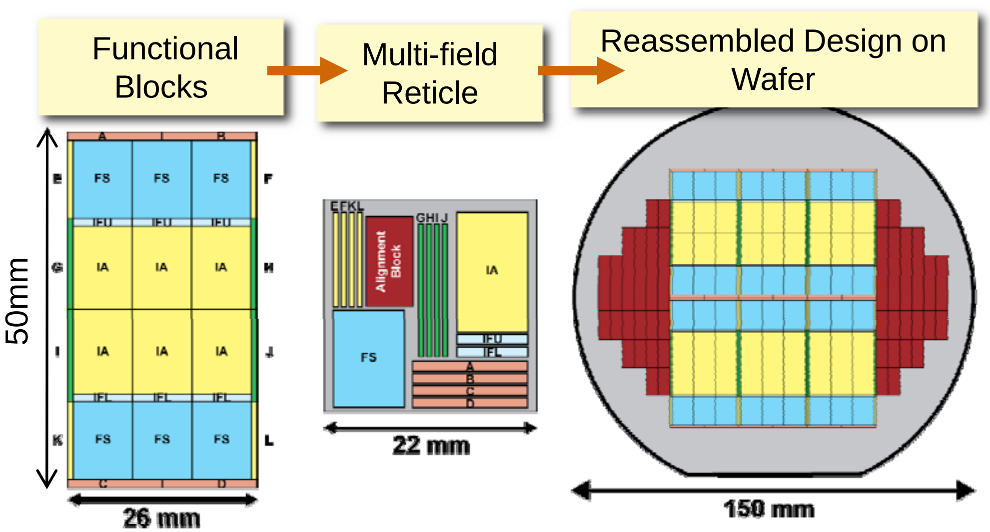
- **Partially populated GPC2 with BI OTAs from 150-mm lots**
- **200-mm wafer OTA process in development**
  - Fe^{55} X-rays detected with first FI devices

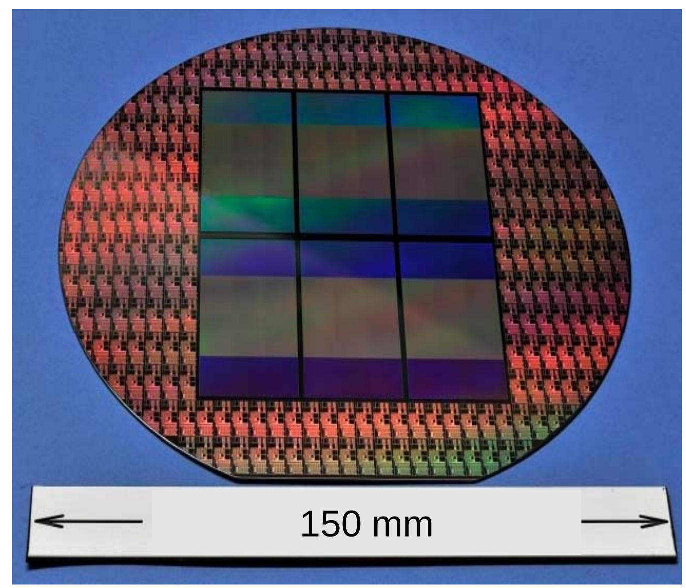




Stitched Large Format Arrays

- **Stitching is used when imager size exceeds lithography exposure field**
  - **DUV Stitching methods achieved 35-nm (3σ) precision**
- **Mix-and-Match is used to combine fine-line (90 nm) Front End of Line lithography with thick, wide routing metals in Back End of Line steps**
  - **In use for 3-D integrated imagers**

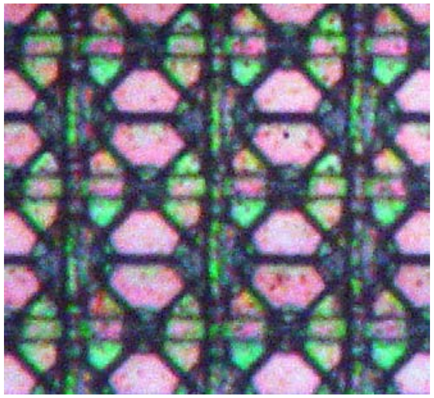




New Process Technology for OTCCDs

Current process

- **Four polysilicon layers**
- **Clock voltages: 8 – 10 V**
- **Pixel sizes > 9 µm**

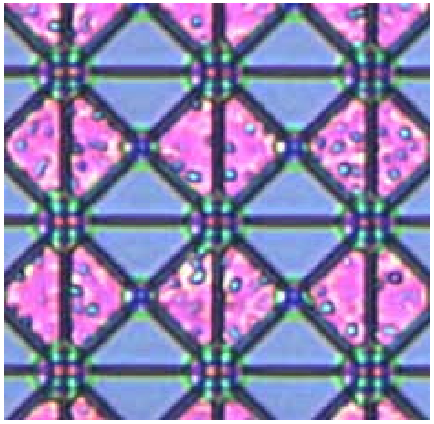


10-µm pixels
(four poly layers)

Advanced process

- **Single or Two polysilicon layers**
- **Clock voltages: down to 2 V**
- **Pixel sizes > 5 µm**

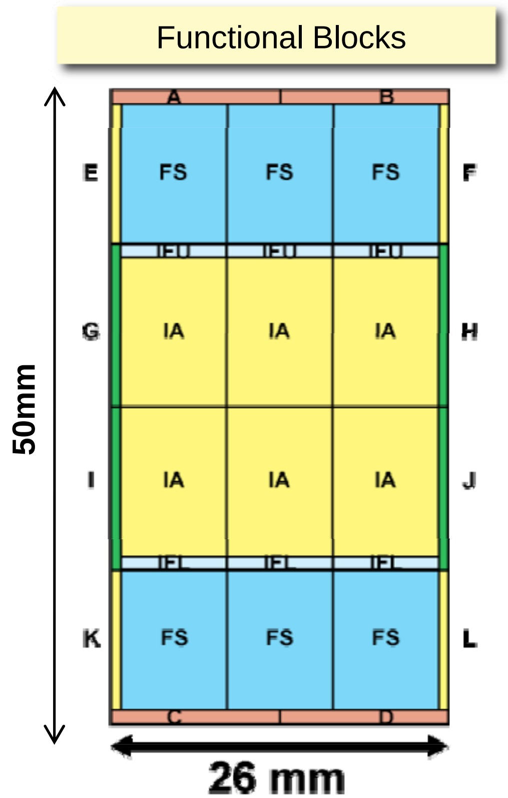
➡ ***Simplified fabrication but requires sub-µm lithography***



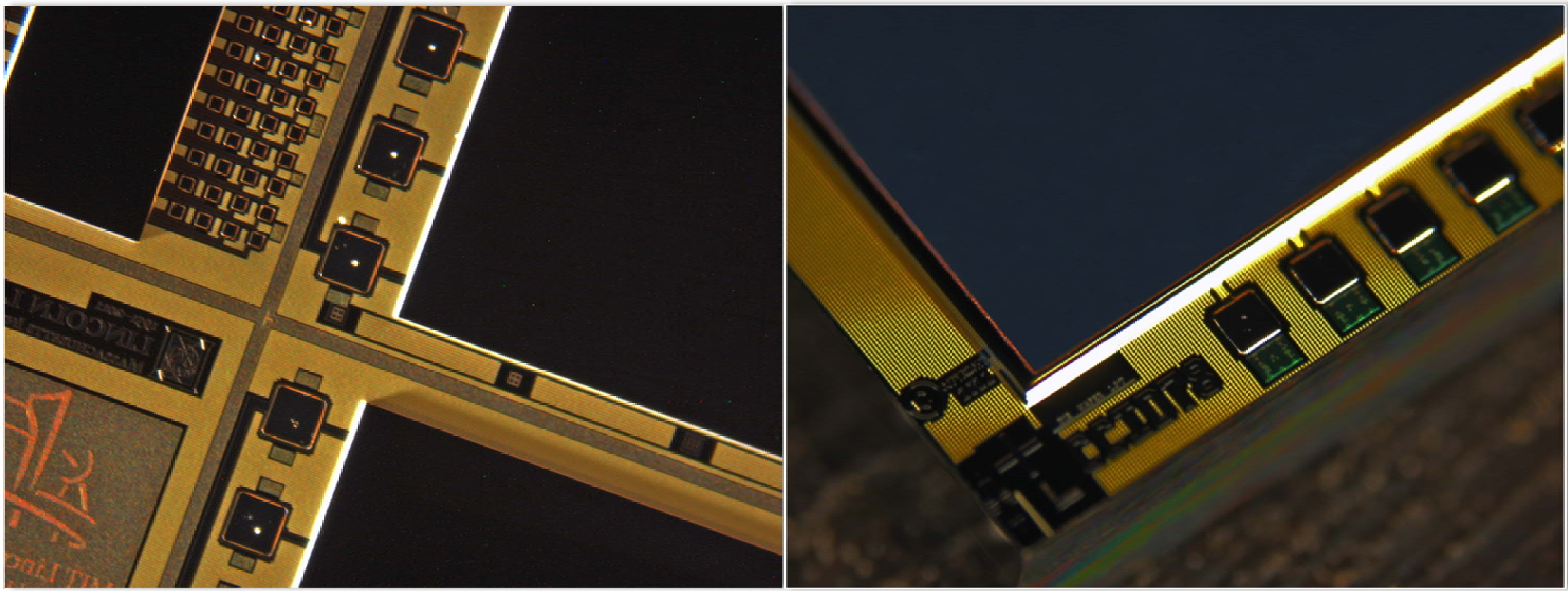
8-µm pixels
(two poly layers)

Collection of Fe^{55} X-ray Events in IA
3k x 3k, 8-µm pixel OTCCD

Fe55 events captured throughout Imaging array

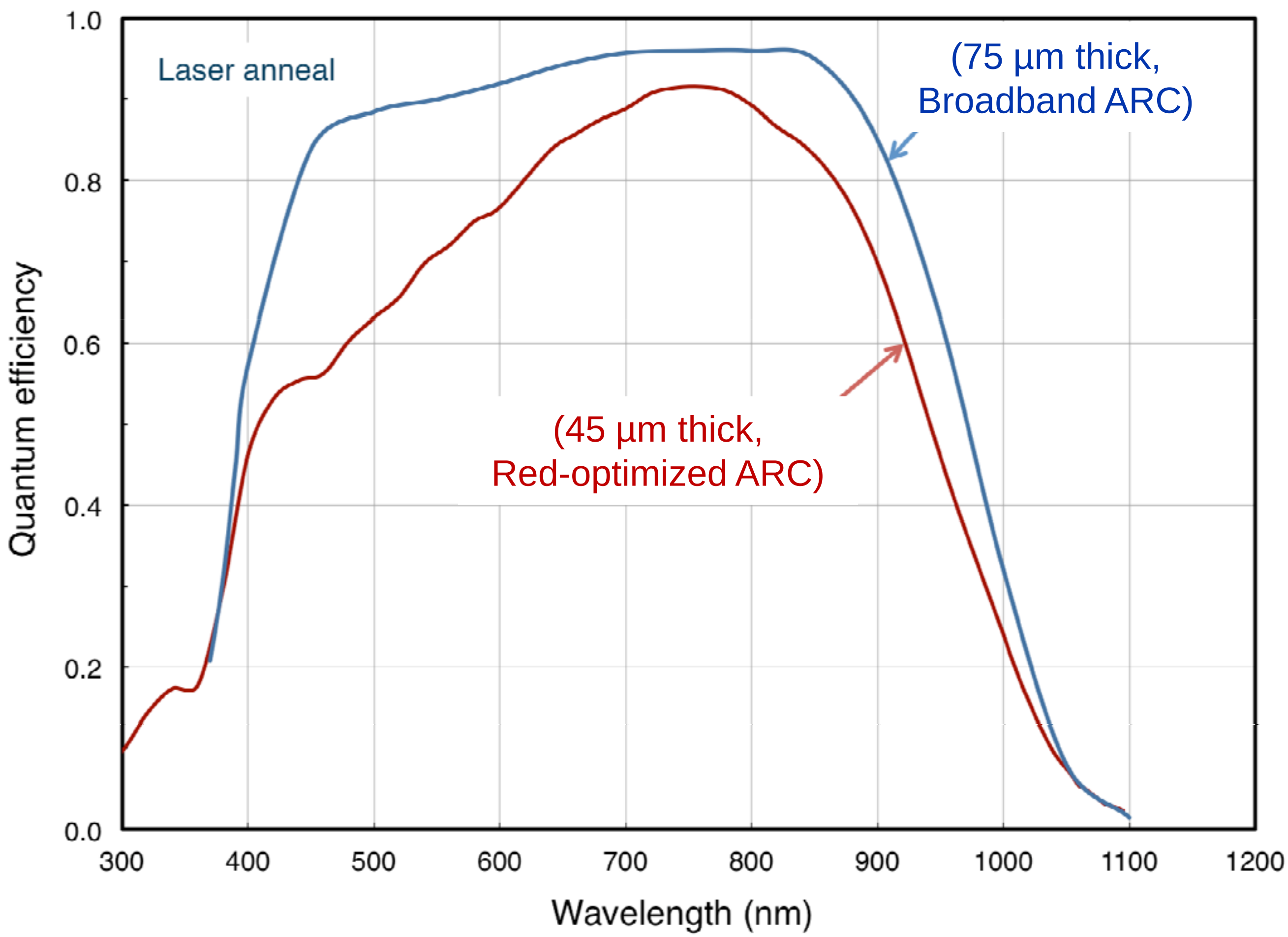


Completed Back-Illuminated Devices



Chip Photomicrograph Details

QE of Back-Illuminated Devices
Effect of Detector Thickness

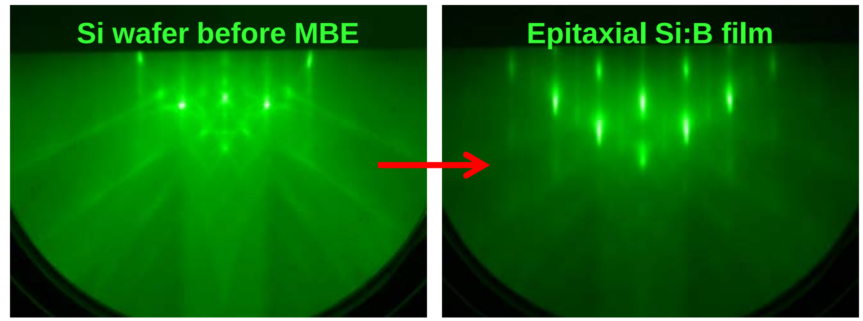


Minimizing Dead Layers Through MBE

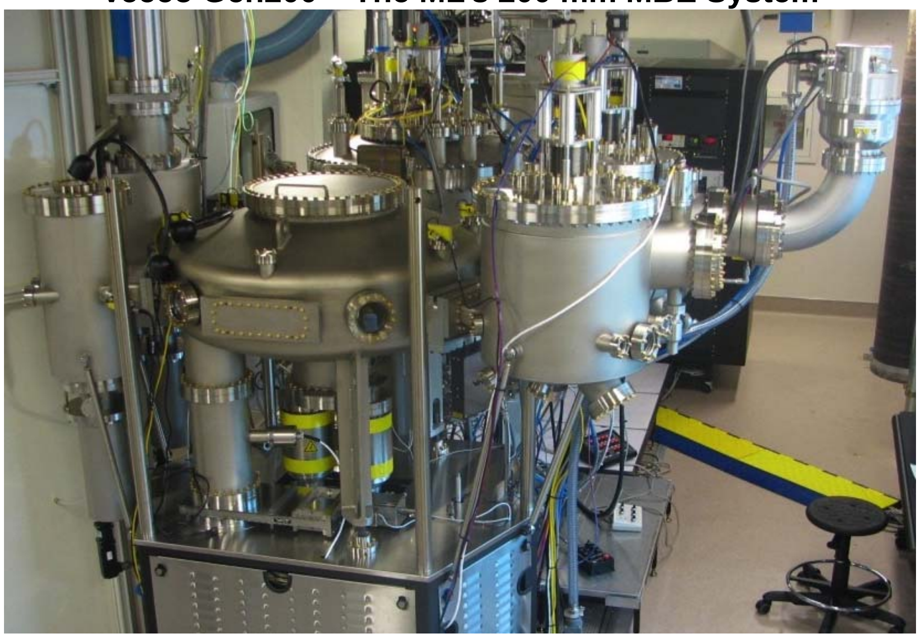
- MBE enables the growth of ultra-thin (5-10 nm) Si:B passivation layers for BI-CCDs
  - Very low dark current
  - High spatial uniformity
  - Quantum-limited UV detection efficiency

200-mm wafer MBE process successfully demonstrated

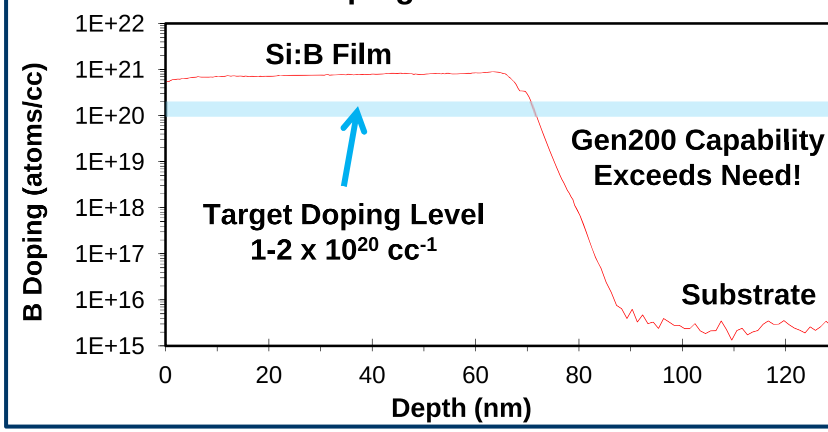
In situ **e^- diffraction images show epitaxial film growth**



Veeco Gen200 – The ML's 200 mm MBE System

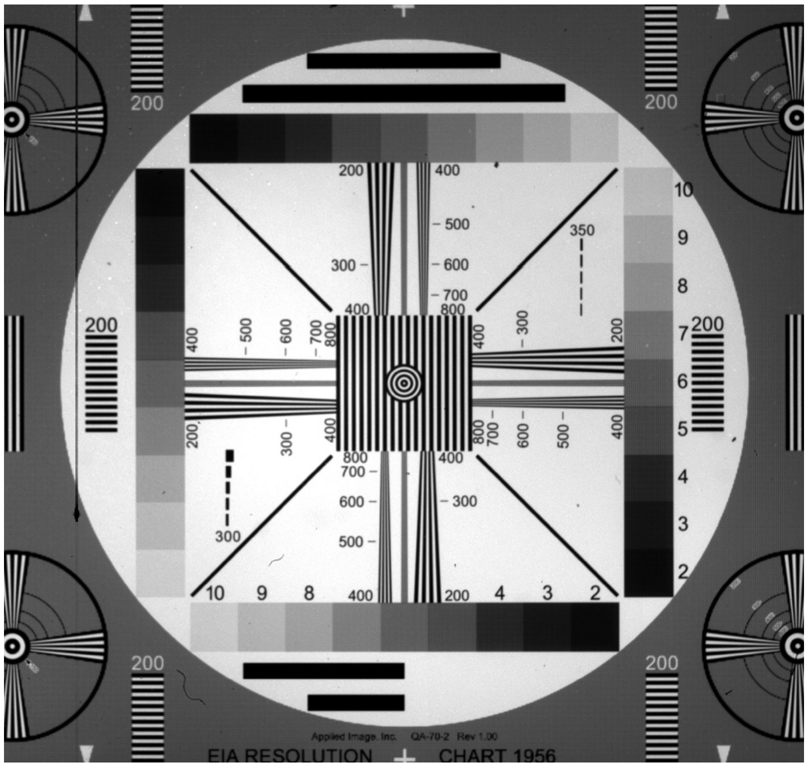


Si:B Doping Profile – 200 mm Wafer



Completed MBE-Treated Devices

430nm LED Resolution Target

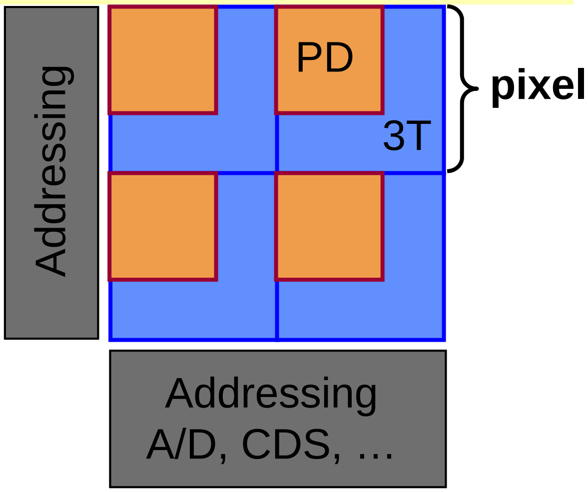


Fe55 Single Pixel events at -50C

Charge Transfer Inefficiency< 10^{-6}

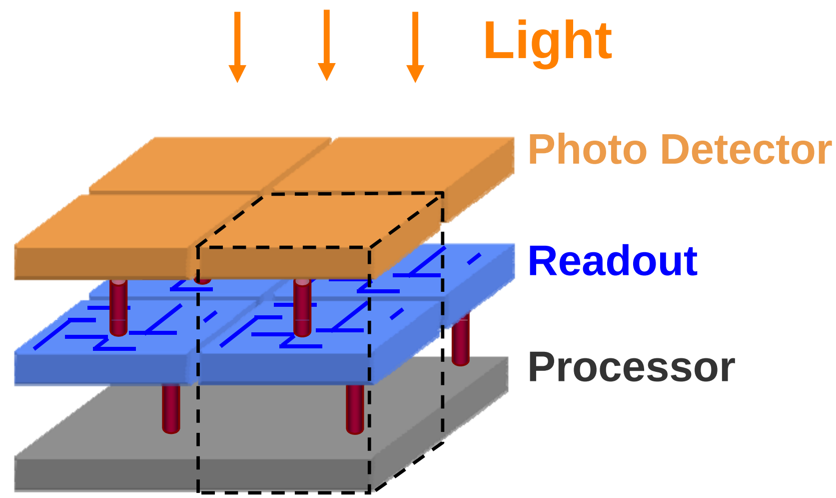
Advantages of 3-D IC for Advanced Focal Planes

Conventional Monolithic CMOS Image Sensor



- **Pixel electronics and detectors share area**
- **Control and support electronics placed outside of imaging area**
- **Fill factor loss**
- **Co-optimized fabrication**

3-D Pixel

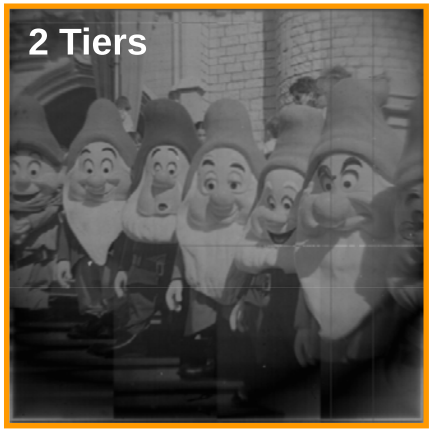


- **100% fill factor detector**
- **Fabrication optimized by layer function**
- **Local image processing**
- **Scalable to large-area focal planes**

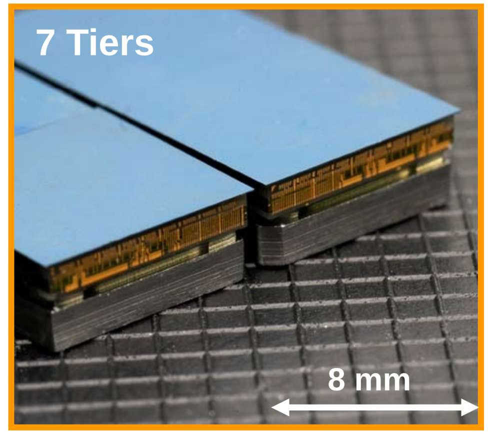
3-D Imager Demonstrations at MIT-LL

CMOS Imagers for Daylight Applications

CMOS Image Sensor
(IEEE ISSCC 2005)

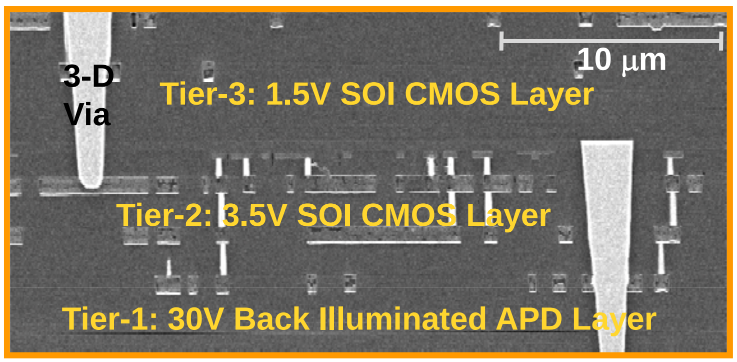


Four-side Abuttable CMOS APS
(IEEE ISSCC 2009)

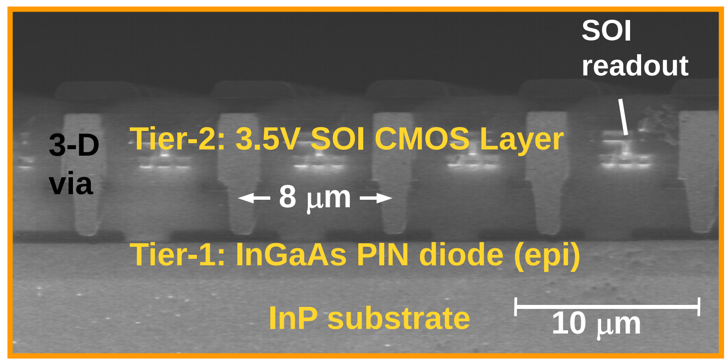


Mixed Material/Process Imagers

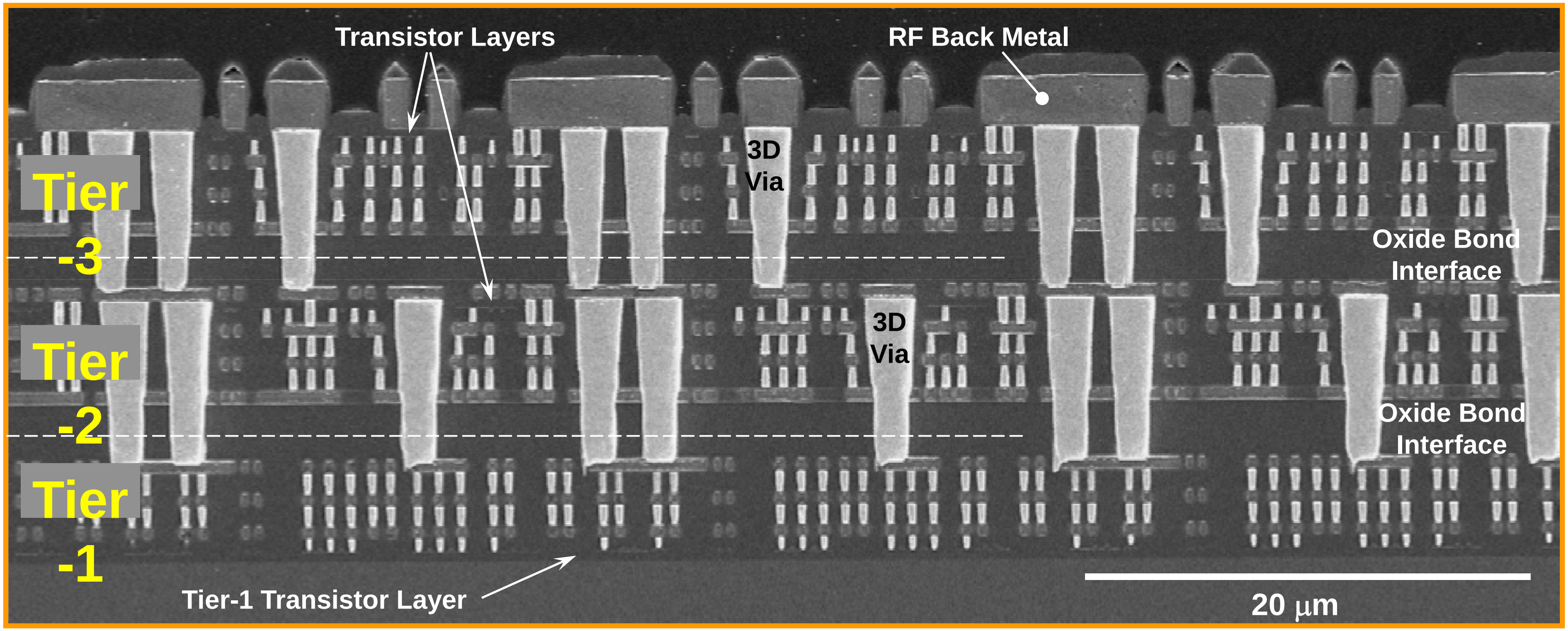
GmAPD Laser Radar
(IEEE ISSCC 2006)



InGaAs Detector
(IEEE 3DIC 2009)



3-Tier 3DIC Cross-Section



Three FDSOI CMOS Tiers, total active circuit height ~ 21 um

Tier 1 bottom, Tier 2 and Tier 3 inverted and bonded on top, substrates removed

11 metal interconnect layers thick RF top metal

Dense unrestricted 3D vias for electrical connections between tiers

Summary

- **Lincoln Laboratory is now fabricating scientific detectors on 200-mm silicon substrates**
  - **Stitching to produce very large format devices**
  - **Uniform response and broad-band sensitivity**
  - **Advancements in Back Illumination technology**
- **Ongoing work to design and fabricate new designs for adaptive optics applications**
- **Increased on-focal plane processing anticipated with next generation 3-D integrated circuit technologies**

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