Developments in CCD and CMOS Detectors at MIT Lincoln Laboratory

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Scientific Detector Workshop
7 October 2013
MIT Lincoln Laboratory

- Federally-Funded Research and Development Center (FFRDC) run by the Massachusetts Institute of Technology under contract with the Air Force. Located on Hanscom Air Force Base in Lexington, MA
  - ~3800 employees
  - ~$940M/yr (FY12) sponsored research

- Primary focus is on the development of prototype radar, communications, and surveillance systems for the DoD and other government agencies
  - Conduct research in advanced electronics technology to support and enable new prototype system development
  - Growing segment in industrial-sponsored research through CRDA

- Work with US industry to transfer Lincoln Laboratory technology to meet future DoD and government needs
Unique Focal-Plane Technology in Support of National Security

AMOS (AF)
DoD Satellites
Directed Energy AFRL SOR
Space Surveillance
Laser Radar
Astronomy
National Ignition Facility (LLNL)
Nuclear Stockpile Stewardship (LANL)
Microelectronics Laboratory

- Specially designed 70,000 square foot building
  - First completed silicon (Spring 1993)
  - Converted to 150 mm wafer processing in 1996
  - Converted to 200 mm wafer processing (Spring 2011)

- Clean Room space
  - 8,100 Square feet of class-10
  - 10,000 Square feet of class-100

- Microelectronics Laboratory activities
  - > 30 Active programs in support of 4 divisions
  - > 65 People from 5 groups working full-time in facility (Scientists, Engineers, and Technicians)
  - Two-shift operation, 6 am to 11 pm, 5 days/week

Facility/Equipment Value ~$175-200M
Spanning Research to Low-Volume Prototyping in One Facility

Graphene Devices

22M-pixel Orthogonal Transfer Array Focal Plane Tiles

MEMS RF Switches

MASIVS Focal Plane Array

9-nm Gate-Length Fully Depleted SOI

InP/CMOS 3-D Integration of SWIR FPA

Curved CCD Focal Plane Arrays for Space Surveillance Telescope

Device Research/ Novel Materials

Demonstration Circuits/Devices

Low volume, specialized, sophisticated prototypes
Growth in Wafer and Device Sizes

- **Wafer area**
- **Largest Lincoln Imagers**
- **Digital SLR sensors**
- **Compact cameras**
- **Cell-phone cameras**

![Graph showing the growth in wafer and device sizes over time from 1975 to 2020.](image-url)

- Microelectronics Lab opened
- Wafer area
- Largest Lincoln Imagers

Year:
- 1975
- 1980
- 1985
- 1990
- 1995
- 2000
- 2005
- 2010
- 2015
- 2020

Area (cm²):
- 0.1
- 1.0
- 10.0
- 100.0
- 1000.0

MITLL SDW 2013-6
VS 10/07/13
## Existing Sensors for Adaptive Optics

<table>
<thead>
<tr>
<th>Device</th>
<th>Format (Ports)</th>
<th>Pixel Size</th>
<th>Frame Rate</th>
<th>Read Noise</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCID26</td>
<td>$128 \times 128$ (16)</td>
<td>21 μm</td>
<td>2.5 kfps</td>
<td>7 e⁻</td>
<td>Electronic shutter</td>
</tr>
<tr>
<td>CCID66</td>
<td>$160 \times 160$ (20)</td>
<td>21 μm</td>
<td>2.5 kfps</td>
<td>4 e⁻</td>
<td>High-responsivity pJFET charge-sense with two-stage on-chip amplification</td>
</tr>
</tbody>
</table>

**Die Photo MITLL CCID26**

**Die Photo MITLL CCID66**
Photomicrograph Detail of Wafer
Evolutionary Technology
Enhance NIR Sensitive AO CCD

**Sensors for Adaptive Optics**

- MIT-LL CCID75: Adaptive Optics CCD with readout port isolation and region-of-interest for high-frame-rate / low-latency operation

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Size</td>
<td>160 × 160</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>21 µm</td>
</tr>
<tr>
<td>Well Depth</td>
<td>&gt; 50,000 e⁻</td>
</tr>
<tr>
<td>Wavelength</td>
<td>0.4 – 1.1 µm</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>2.5 kfps</td>
</tr>
</tbody>
</table>

CCID75 Photograph

**CCID75**

DISTRIBUTION C. Distribution authorized to U.S. Government Agencies and their contractors; Specific Authority (AFRL/RD Critical Information List) 20130920. Other requests shall be referred to AFRL/RDSA, 3550 Aberdeen Avenue SE, Kirtland AFB, NM 87117-5776.
Targeted Technology
Polar Coordinate Imager

Sensors for Adaptive Optics

• Example: Polar coordinate imaging to address the challenge of Adaptive Optics for extremely-large telescopes

Sodium beacon images

• Sodium beacon image elongates radially as the distance from center of the focal plane increase
• Many small CCD arrays located and oriented to optimally sample each sub-aperture
Front illumination test results

<table>
<thead>
<tr>
<th>Device</th>
<th>L1-W1-C3</th>
<th>L1-W3-C1</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read noise</td>
<td>3.47</td>
<td>3.24</td>
<td>e-</td>
</tr>
<tr>
<td>Full well</td>
<td>26844</td>
<td>24967</td>
<td>e-</td>
</tr>
<tr>
<td>Non-linearity</td>
<td>1.2</td>
<td>1.4</td>
<td>%</td>
</tr>
<tr>
<td>Responsivity</td>
<td>15</td>
<td>16</td>
<td>μV/e-</td>
</tr>
<tr>
<td>Dark current</td>
<td>~10*</td>
<td>~2.1</td>
<td>e-/pixel/s</td>
</tr>
<tr>
<td>Serial CTE</td>
<td>0.999991</td>
<td>0.999993</td>
<td>-</td>
</tr>
<tr>
<td>Parallel CTE</td>
<td>0.999990</td>
<td>0.999990</td>
<td>-</td>
</tr>
<tr>
<td>Charge diffusion</td>
<td>0.25</td>
<td>0.37</td>
<td>pixels</td>
</tr>
</tbody>
</table>

* = device operated at -8 °C

- L1-W1-C3 was not baked and has an epoxy seal
- Later determined devices were operating at ~ -15 °C and ~ -29 °C
### Device L1-W1-C3

<table>
<thead>
<tr>
<th>Video channel</th>
<th>Average</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
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<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
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<tbody>
<tr>
<td>Read noise</td>
<td>3.46</td>
<td>3.71</td>
<td>3.73</td>
<td>3.23</td>
<td>2.96</td>
<td>3.61</td>
<td>3.26</td>
<td>3.28</td>
<td>3.71</td>
<td>3.70</td>
<td>3.54</td>
<td>3.69</td>
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<td>3.28</td>
<td>3.32</td>
<td>3.35</td>
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<tr>
<td>Gain (e-/DN)</td>
<td>0.53</td>
<td>0.56</td>
<td>0.56</td>
<td>0.50</td>
<td>0.48</td>
<td>0.52</td>
<td>0.52</td>
<td>0.55</td>
<td>0.53</td>
<td>0.55</td>
<td>0.54</td>
<td>0.56</td>
<td>0.54</td>
<td>0.53</td>
<td>0.49</td>
<td>0.53</td>
<td>0.56</td>
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<tr>
<td>Full well</td>
<td>26714</td>
<td>26806</td>
<td>25122</td>
<td>25305</td>
<td>27528</td>
<td>25095</td>
<td>24579</td>
<td>28898</td>
<td>26129</td>
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<td>26000</td>
<td>27847</td>
<td>26691</td>
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<table>
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<th>Video channel</th>
<th>Average</th>
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<th>18</th>
<th>19</th>
<th>20</th>
<th>21</th>
<th>22</th>
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<th>29</th>
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<tbody>
<tr>
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<td>3.15</td>
<td>3.60</td>
<td>3.10</td>
<td>3.74</td>
<td>3.63</td>
<td>3.12</td>
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<td>3.79</td>
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<td>Gain (e-/DN)</td>
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<td>0.55</td>
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<td>0.52</td>
<td>0.53</td>
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<td>0.55</td>
<td>0.56</td>
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<tr>
<td>Full well</td>
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<td>26945</td>
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<td>28402</td>
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<td>28108</td>
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<td>26388</td>
<td>27306</td>
<td>24502</td>
<td>28523</td>
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### Device L1-W3-C1

<table>
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<th>14</th>
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<tbody>
<tr>
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<td>3.20</td>
<td>2.83</td>
<td>3.63</td>
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<td>3.54</td>
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<td>3.68</td>
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<td>3.01</td>
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<td>2.77</td>
</tr>
<tr>
<td>Gain (e-/DN)</td>
<td>0.52</td>
<td>0.46</td>
<td>0.50</td>
<td>0.51</td>
<td>0.50</td>
<td>0.51</td>
<td>0.49</td>
<td>0.49</td>
<td>0.45</td>
<td>0.54</td>
<td>0.52</td>
<td>0.56</td>
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<td>0.54</td>
<td>0.57</td>
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<tr>
<td>Full well</td>
<td>25452</td>
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<td>26281</td>
<td>26004</td>
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<td>24779</td>
<td>26802</td>
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<td>27091</td>
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<table>
<thead>
<tr>
<th>Video channel</th>
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<th>17</th>
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<th>20</th>
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</thead>
<tbody>
<tr>
<td>Read noise</td>
<td>3.30</td>
<td>3.57</td>
<td>3.65</td>
<td>2.86</td>
<td>3.75</td>
<td>2.95</td>
<td>2.86</td>
<td>3.49</td>
<td>3.04</td>
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<td>3.71</td>
<td>2.87</td>
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<td>2.95</td>
<td>3.66</td>
<td>3.19</td>
<td>3.64</td>
</tr>
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<td>Gain (e-/DN)</td>
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<td>0.50</td>
<td>0.57</td>
<td>0.47</td>
<td>0.53</td>
<td>0.50</td>
<td>0.54</td>
<td>0.45</td>
<td>0.55</td>
<td>0.53</td>
<td>0.56</td>
<td>0.56</td>
<td>0.52</td>
<td>0.51</td>
<td>0.50</td>
<td>0.50</td>
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<tr>
<td>Full well</td>
<td>24482</td>
<td>23327</td>
<td>25106</td>
<td>22943</td>
<td>23667</td>
<td>23141</td>
<td>24771</td>
<td>23276</td>
<td>26526</td>
<td>25514</td>
<td>26141</td>
<td>25086</td>
<td>25412</td>
<td>24347</td>
<td>25053</td>
<td>23157</td>
<td>24247</td>
</tr>
</tbody>
</table>
Transition from 150-mm to 200-mm Wafers

SVG i-line Scanner
1× scanner (150-mm field)
~500 nm overlay typ.
2-µm resolution typ.

Canon i-line Stepper (0.25 NA)
< 100-nm overlay
800-nm resolution
2× stepper (> 50 × 50 mm field)
I-line Stepper Lithography
200-mm Wafer Capability Demonstrators

Same Reticle Used

Full Field Stepping  Full Field Stepping  16 CCDs Per Wafer

FI = Front Illuminated

150 mm  200 mm  200 mm
Results from First 200-mm CCD Lot
3k x 3k Image Array and Frame Store (9.5µm pixel)
Uniformity of Large Area CCDs

FI 3k x 3k

BI 1k x 2k

Output Circuits

60 sec integration at -20°C

BICCID-78 L1a-W1-C7 Imaging Array at -30°C using 430 nm LED

20-port Adaptive Optics Device CCID75

+/- 1%
Orthogonal Transfer Arrays for Pan-STARRS GPC2

- Device Improvements (CCID71)
  - Improved video quality by using only 2-phase devices
  - Increased full well
  - Improved fill factor
  - Reduced persistence and amplifier glow
  - Better AR coating

- Partially populated GPC2 with BI OTAs from 150-mm lots

- 200-mm wafer OTA process in development
  - Fe$^{55}$ X-rays detected with first FI devices
Stitched Large Format Arrays

- Stitching is used when imager size exceeds lithography exposure field
  - DUV Stitching methods achieved 35-nm (3σ) precision
- Mix-and-Match is used to combine fine-line (90 nm) Front End of Line lithography with thick, wide routing metals in Back End of Line steps
  - In use for 3-D integrated imagers
New Process Technology for OTCCDs

Current process
• Four polysilicon layers
• Clock voltages: 8 – 10 V
• Pixel sizes > 9 µm

Advanced process
• Single or Two polysilicon layers
• Clock voltages: down to 2 V
• Pixel sizes > 5 µm

➡ Simplified fabrication but requires sub-µm lithography

10-µm pixels
(four poly layers)

8-µm pixels
(two poly layers)
Collection of $^{55}$Fe X-ray Events in IA

3k x 3k, 8-µm pixel OTCCD

Fe55 events captured throughout Imaging array

Functional Blocks

50mm

26 mm
Completed Back-Illuminated Devices

Chip Photomicrograph Details
QE of Back-Illuminated Devices
Effect of Detector Thickness

![Graph showing quantum efficiency versus wavelength for two different thicknesses and ARC optimizations.](image.png)

- Laser anneal (75 µm thick, Broadband ARC)
- (45 µm thick, Red-optimized ARC)
Minimizing Dead Layers Through MBE

- MBE enables the growth of ultra-thin (5-10 nm) Si:B passivation layers for BI-CCDs
  - Very low dark current
  - High spatial uniformity
  - Quantum-limited UV detection efficiency

200-mm wafer MBE process successfully demonstrated

*In situ* e- diffraction images show epitaxial film growth

Veeco Gen200 – The ML’s 200 mm MBE System

Si:B Doping Profile – 200 mm Wafer

<table>
<thead>
<tr>
<th>Depth (nm)</th>
<th>B Doping (atoms/cc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1E+15</td>
</tr>
<tr>
<td>20</td>
<td>1E+16</td>
</tr>
<tr>
<td>40</td>
<td>1E+17</td>
</tr>
<tr>
<td>60</td>
<td>1E+18</td>
</tr>
<tr>
<td>80</td>
<td>1E+19</td>
</tr>
<tr>
<td>100</td>
<td>1E+20</td>
</tr>
<tr>
<td>120</td>
<td>1E+21</td>
</tr>
<tr>
<td>120</td>
<td>1E+22</td>
</tr>
</tbody>
</table>

Si:B Film

Target Doping Level
1-2 x 10²⁰ cc⁻¹

Gen200 Capability Exceeds Need!

Substrate
Completed MBE-Treated Devices

430nm LED Resolution Target

Fe55 Single Pixel events at -50C

Charge Transfer Inefficiency < 10^{-6}
Advantages of 3-D IC for Advanced Focal Planes

Conventional Monolithic CMOS Image Sensor

- Pixel electronics and detectors share area
- Control and support electronics placed outside of imaging area
- Fill factor loss
- Co-optimized fabrication

3-D Pixel

- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
- Scalable to large-area focal planes

MITLL SDW 2013-25
VS 10/07/13
# 3-D Imager Demonstrations at MIT-LL

<table>
<thead>
<tr>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Tier-1: 30V Back Illuminated APD Layer</td>
<td>Tier-3: 1.5V SOI CMOS Layer</td>
<td>Tier-2: 3.5V SOI CMOS Layer</td>
</tr>
<tr>
<td>Tier-2: 5.5V SOI CMOS Layer</td>
<td></td>
<td>Tier-1: InGaAs PIN diode (epi)</td>
</tr>
<tr>
<td>Tier-3: 1.5V SOI CMOS Layer</td>
<td></td>
<td>InP substrate</td>
</tr>
</tbody>
</table>

## Mixed Material/Process Imagers

- **GmAPD Laser Radar (IEEE ISSCC 2006)**
- **InGaAs Detector (IEEE 3DIC 2009)**
Three FDSOI CMOS Tiers, total active circuit height ~ 21 um
Tier 1 bottom, Tier 2 and Tier 3 inverted and bonded on top, substrates removed
11 metal interconnect layers thick RF top metal
Dense unrestricted 3D vias for electrical connections between tiers
Summary

• Lincoln Laboratory is now fabricating scientific detectors on 200-mm silicon substrates
  – Stitching to produce very large format devices
  – Uniform response and broad-band sensitivity
  – Advancements in Back Illumination technology

• Ongoing work to design and fabricate new designs for adaptive optics applications

• Increased on-focal plane processing anticipated with next generation 3-D integrated circuit technologies
Acknowledgements

• The Lincoln Laboratory, Massachusetts Institute of Technology
  – Brian Aull, Barry Burke, Michael Cooper, Brad Felton, Jim Gregory, Renee Lambert, Dan O’Mara, Robert Reich, Dan Schuette, Doug Young, and members of the Advanced Imagers and Silicon Technology Group

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  – Robert Johnson, John Wynia

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  – Sean Adkins, James W. Beletic, Barry Burke, Charlie Bleau, Jerry Nelson, Ray DuVarney, Richard Stover and Francois Rigaut

• Pan-STARRS Project Collaborators
  – John Tonry, Will Burgett, Peter Onaka

• The TMT Project Office
  – Corrine Boyer, Brent Ellerbroek