A Quantum Computer Architecture Perspective: Executing Quantum Applications on Real Quantum Processors

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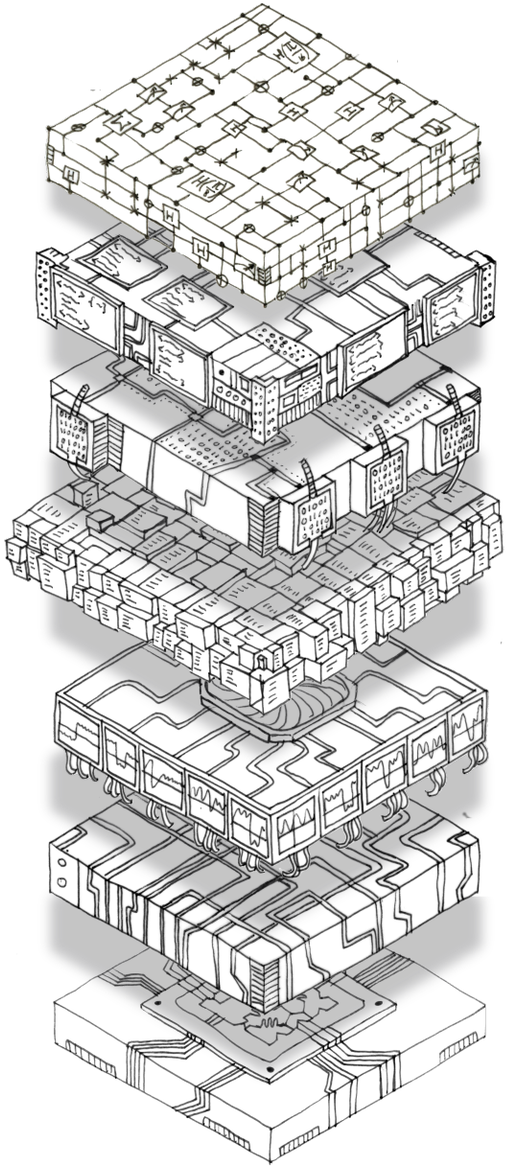

RITphotonics for Quantum.2
July 6, 2020

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QuTech: FT QC roadmap

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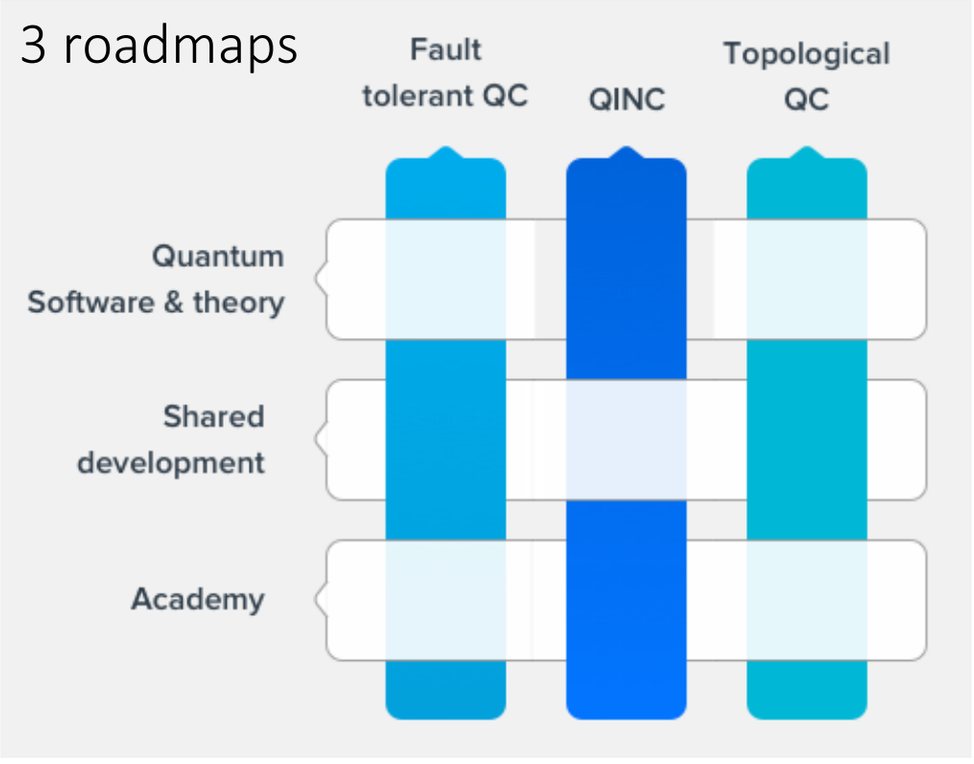

Fault tolerant QC roadmap

The Fault-Tolerant Quantum Computing roadmap aims for a full-stack scalable quantum computing system, including the qubit circuits, the control electronics, and the software layers such as compilers. The approach to achieve fault tolerance is based on quantum error correction, in which information is encoded redundantly enabling error detection without destroying quantum data. The qubit hardware systems are electron spins in quantum dots and superconducting quantum circuits.

Close collaboration with Intel Corporation since 2015

https://qutech.nl

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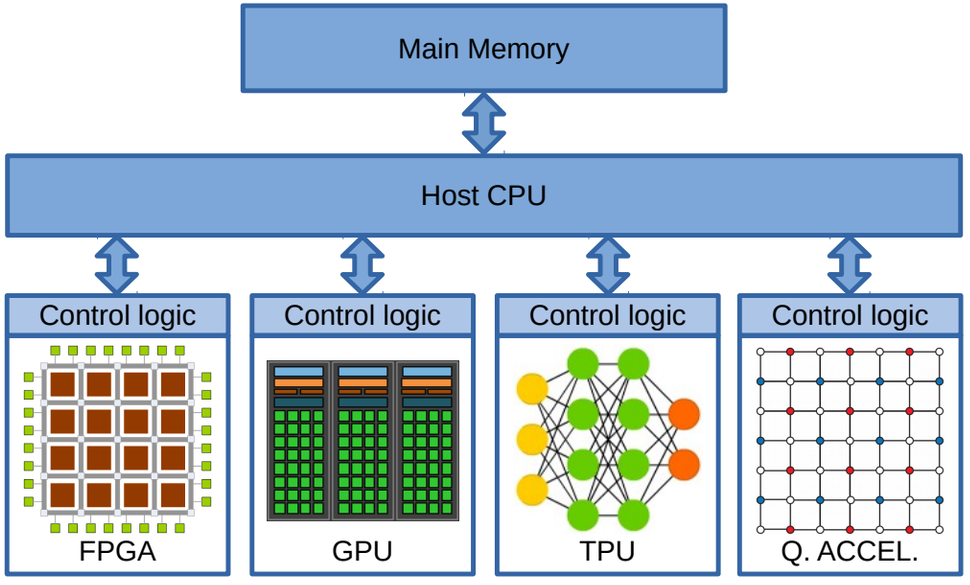
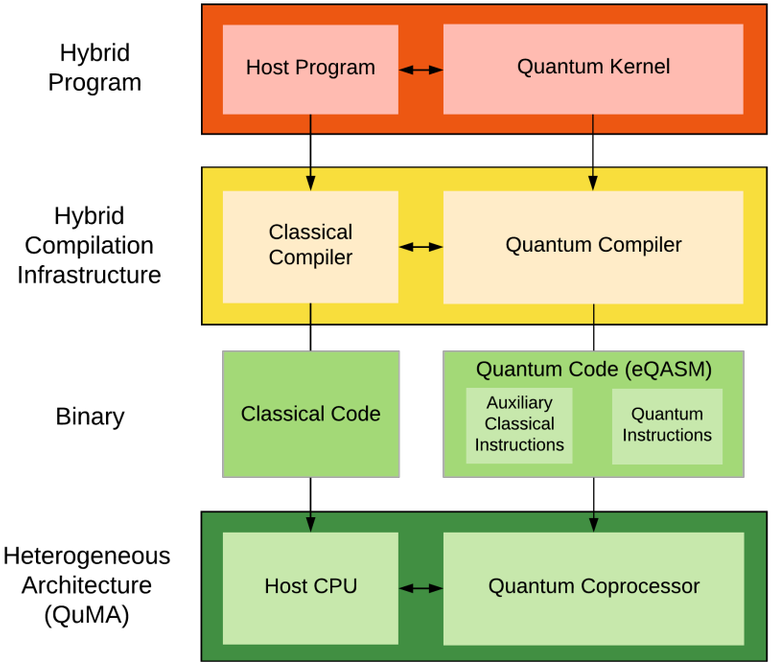
A quantum computer is not (is)

- It is not a replacement for classical computers
- It is an in-memory-computing device
- It is a co-processor in a (heterogeneous) multi-core architecture





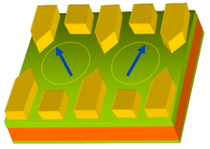
X. Fu et. al, “eQASM: An Executable Quantum Instruction Set Architecture”, *IEEE International Symposium on High Performance Computer Architecture (HPCA), 2019*.

Riesebos, L., et al. "Quantum Accelerated Computer Architectures." *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019.

Where is QC now?

Majoranas (Microsoft)

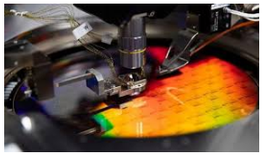
Quantum dots (Intel)



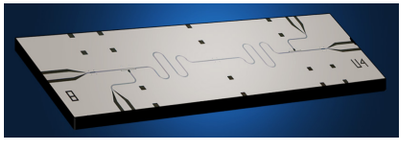
P.W. Shor, "Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer," SIAM Journal on Computing, vol. 26, pp. 1484–1509, 1999.

Shor's algorithm

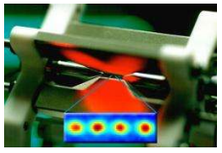
Photonics (PsiQ)



Superconducting (Google, Intel, IBM, Rigetti, Alibaba)



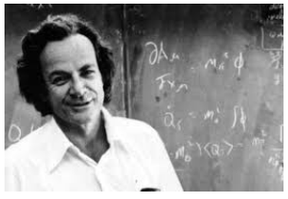
Trapped ions (IonQ)



1994-1995

2012- present

1981



1998-2000

Quantum annealing

Google: 54 (72) qubits
Rigetti: 19 (128) qubits
IBM: 20 (50) qubits
Alibaba: 11 qubits
Intel: 49 qubits

"Can physics be simulated by a universal computer?"

"…the problem is, how can we simulate the quantum mechanics?"

"Can you do it with a new kind of computer - a quantum computer?"

R. P. Feynman, "Simulating physics with computers," International Journal of Theoretical Physics, vol. 21, p. 467–488, 1982.

NISQ era

The noise will place serious limitations on what quantum devices can achieve in the near term.

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Where is QC now?

Coherence times and gate error rates

EXHIBIT 7 | Overview of Leading Quantum Computing Technologies During the NISQ Era

	Leading technologies in NISQ era[1]		Candidate technologies beyond NISQ		
Qubit type or technology	**Superconducting[2]**	**Trapped ion**	**Photonic**	**Silicon-based[3]**	**Topological[8]**
Description of qubit encoding	Two-level system of a superconducting circuit	Electron spin direction of ionized atoms in vacuum	Occupation of a waveguide pair of single photons	Nuclear or electron spin or charge of doped P atoms in Si	Majorana particles in a nanowire
Physical qubits[4,5]	IBM: 20, Rigetti: 19, Alibaba: 11, Google: 9	Lab environment: AQT[6]: 20, IonQ: 14	**6×3**[9]	**2**	target: 1 in 2018
Qubit lifetime	**~50–100 µs**	**~50 s**	**~150 µs**	**~1–10 s**	target ~100 s
Gate fidelity[7]	**~99.4%**	**~99.9%**	**~98%**	**~90%**	target ~99.9999%
Gate operation time	**~10–50 ns**	**~3-50 µs**	**~1 ns**	**~1–10 ns**	–
Connectivity	Nearest neighbors	All-to-all	To be demonstrated	Nearest neighbor	–
Scalability	No major road-blocks near-term	Scaling beyond one trap (>50 qb)	Single photon sources and detection	Novel technology potentially high scalability	?
Maturity or technology readiness level	TRL[10] 5	TRL 4	TRL 3	TRL 3	TRL 1
Key properties	Cryogenic operation Fast gating Silicon technology	Improves with cryogenic temperatures Long qubit lifetime Vacuum operation	Room temperature Fast gating Modular design	Cryogenic operation Fast gating Atomic-scale size	Estimated: Long lifetime High fidelities

The Next decade in Quantum Computing – And How to Play
https://www.bcg.com/publications/2018/next-decade-quantum-computing-how-play.aspx

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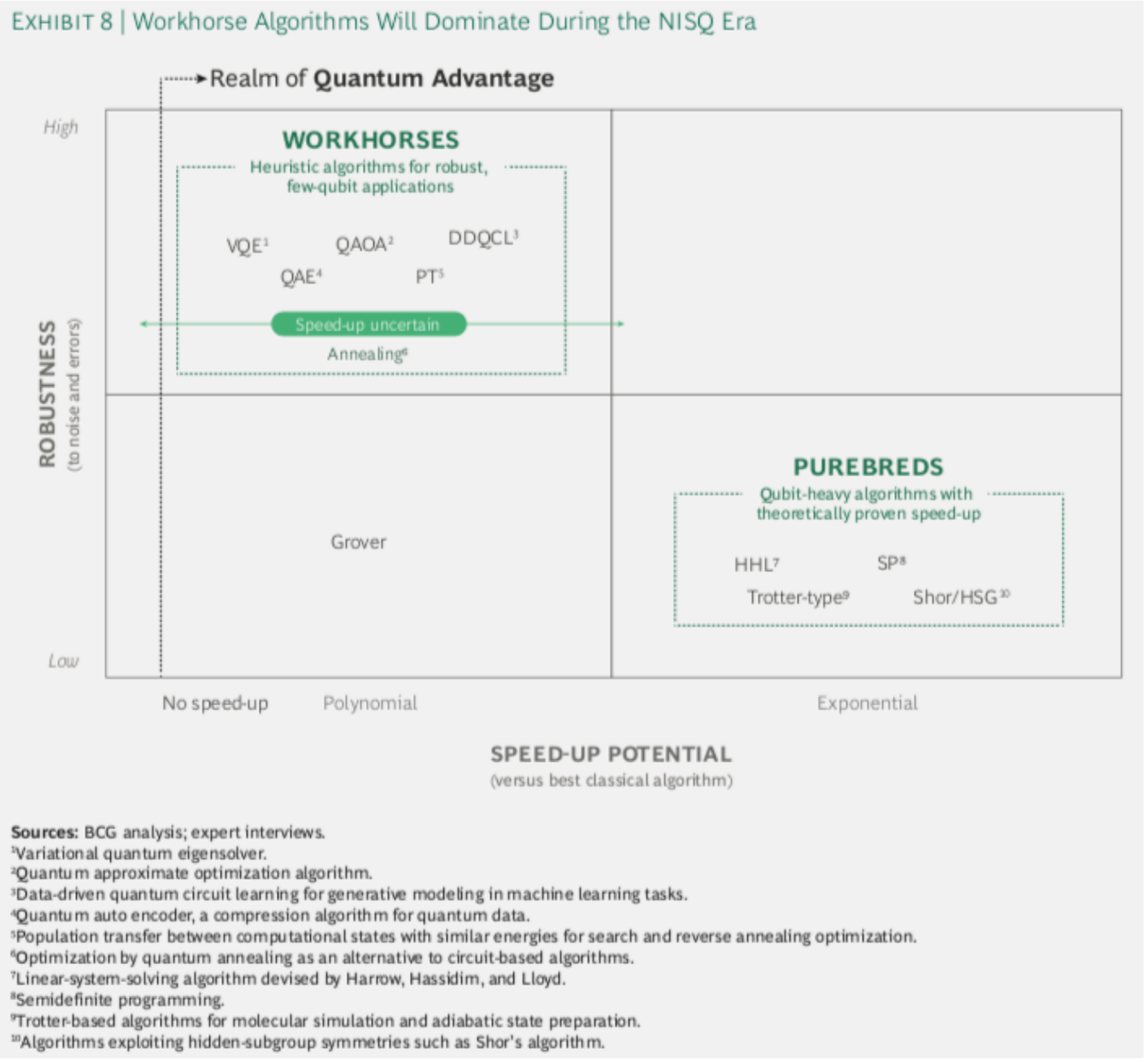
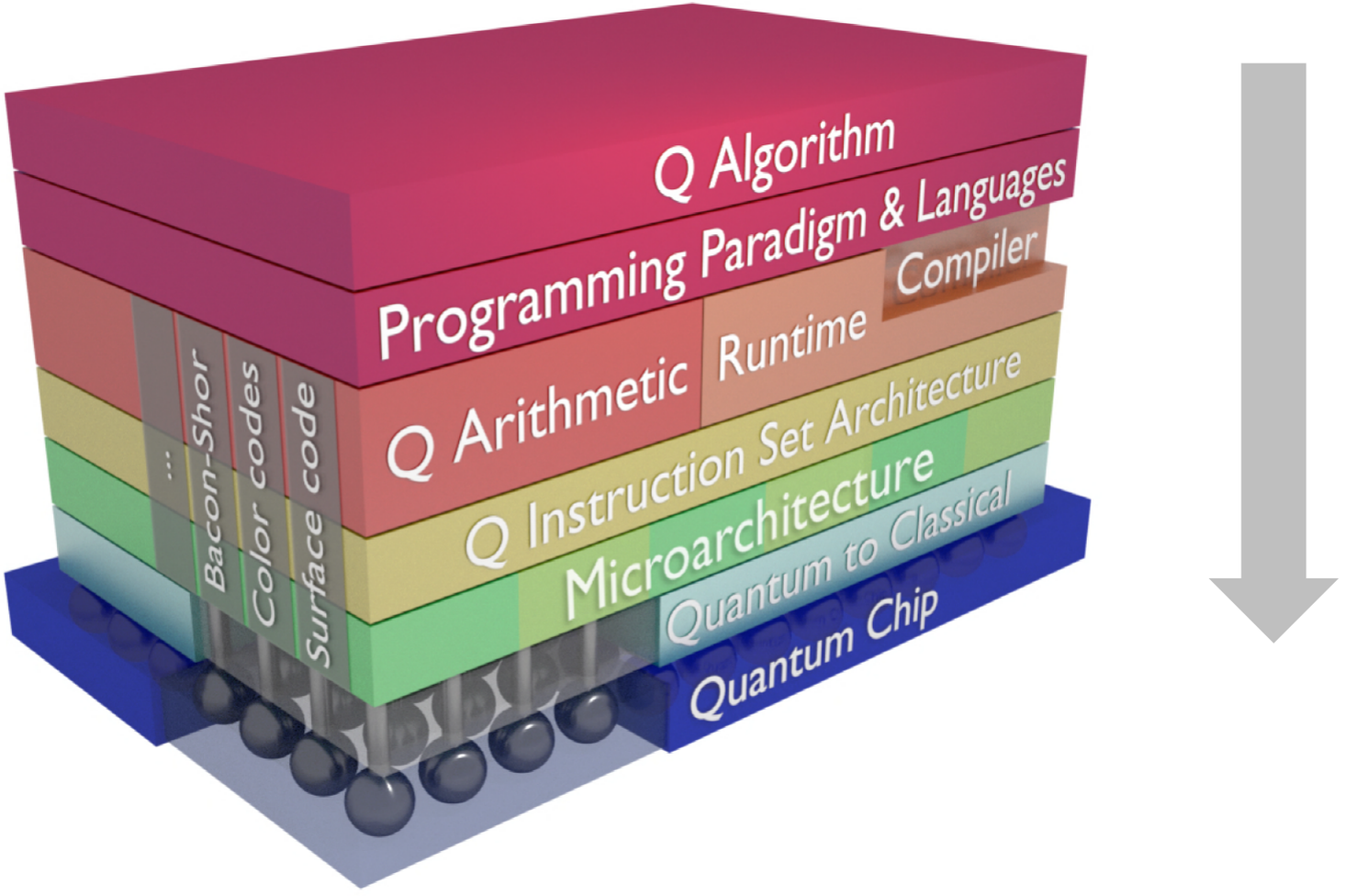


The Next decade in Quantum Computing – And How to Play
https://www.bcg.com/publications/2018/next-decade-quantum-computing-how-play.aspx

Circuit-based quantum computer

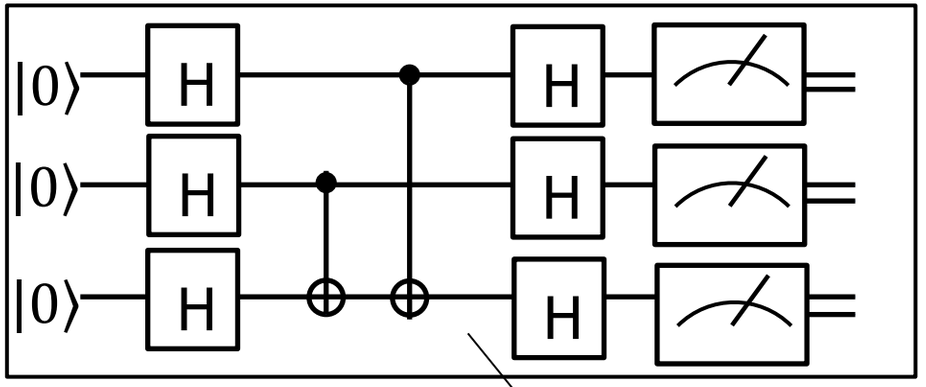


Circuit-based quantum computer

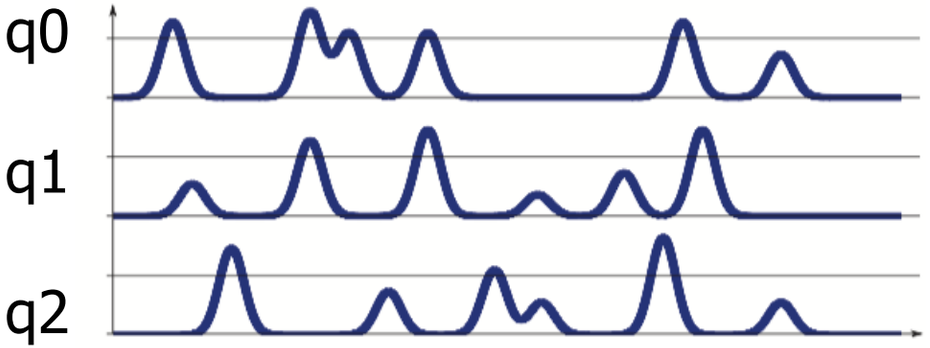
High-level language (Python)

```
qreg = eng.allocate_qureg(3)
Entangle | qureg
Measure | qureg
```

Low-level instructions



Series of pulses



OpenQL (eQASM,cQASM) - TU Delft/Qutech
Quantum Development Kit (Q#) - Microsoft
Quiskit (OpenQASM, OPenPulse) – IBM
Forest (pyQuil,Quil) – Rigetti
ProjectQ (Python, OpenQASM) - ETH Zurich

QASM-like instructions

```
qubit 3
H q0 | H q1
CNOT q1,q2
CNOT q0,q2
H q0 | H q1 | H q2
measure q0 | measure q1 | measure q2
```

K. Khammassi et al. OpenQL: A portable quantum programming framework for quantum accelerators. *arXiv preprint arXiv:2005.13283*, 2020.

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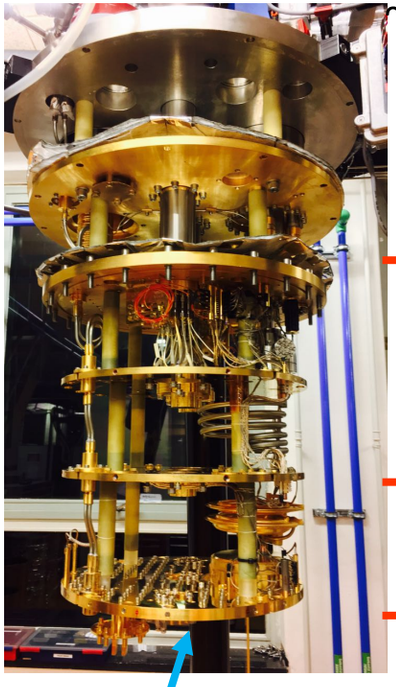
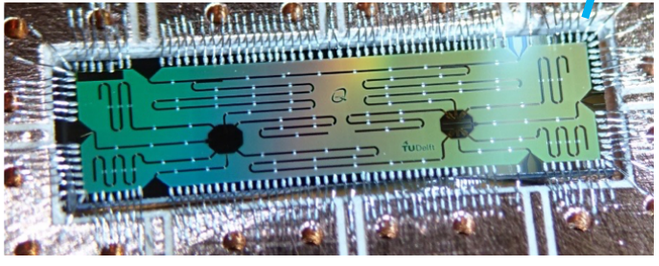
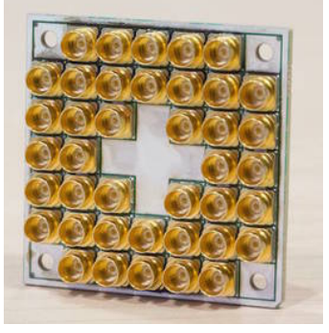
Full-stack implementation

Ground floor

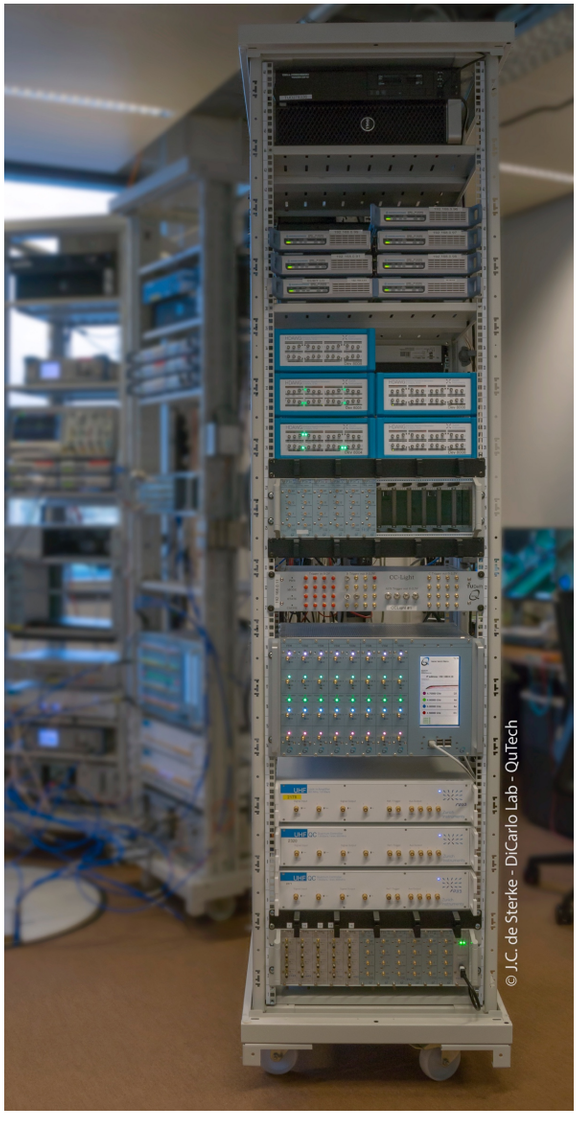




Superconducting quantum processor



First floor



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The multi hardware Quantum Technology platform

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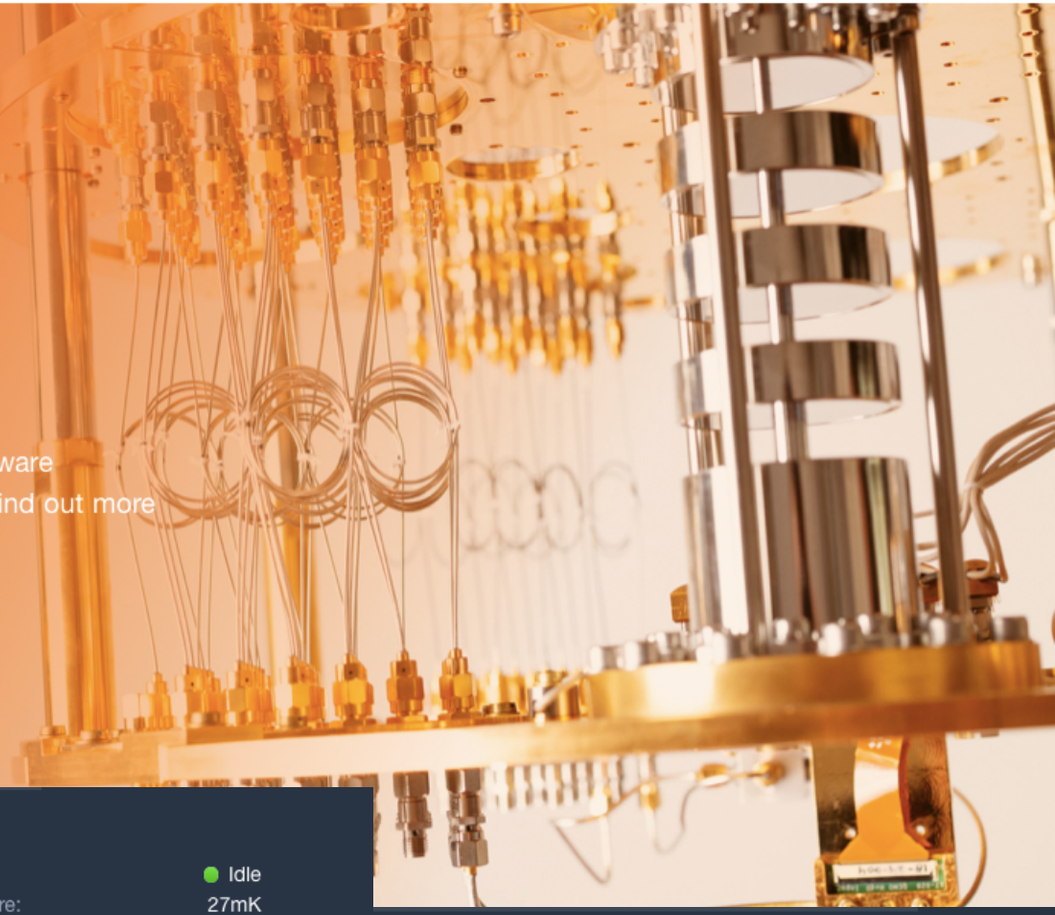

Spin-2

Backend status:
Fridge temperature:
Last calibration date: 5/23/

Learn more

Starmon-5

Backend status: Idle
Fridge temperature: 27mK
Last calibration date: 7/1/2020 - 1:17:12 PM

Learn more

	T1 (µs)	T2e (µs)	F1q (%)	F2q (%)	Finit (%)	FR/O (%)
q0	9.2	15.7	99.8	96.8	99.3	94.5
q1	18.5	11.8	99.6	95.1	97.6	97.4
q2	14.6	24.6	99.8	n.a.	99	98.4
q3	18.1	20.7	99.9	98.1	95	97.3
q4	16.1	23.7	99.9	97.6	99.4	96.3

QX single-node simulator

Backend status: Idle
Number of simulated qubits: 26
Available memory: 4GB
Host: QuTech Delft

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Full-stack challenges

- **Quantum devices**: enhancing coherence, operation fidelity and scalability
- **Control electronics**: Place classical control electronics at cryogenic temperatures.
- **SW-HW co-design:** programming languages, compilers, instruction set architecture and microarchitecture, hybrid classical-quantum computing paradigm

Compilation (mapping) of quantum circuits in NISQ devices

C. G. Almudever et al. "The engineering challenges in quantum computing." *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*.

S. Resch, and U R. Karpuzcu. "Quantum Computing: An Overview Across the System Stack." *arXiv preprint arXiv:1905.07240* (2019).

A.D. Córcoles et. al. ”Challenges and Opportunities of Near-Term Quantum Computing Systems." *arXiv preprint arXiv:1910.02894* (2019).

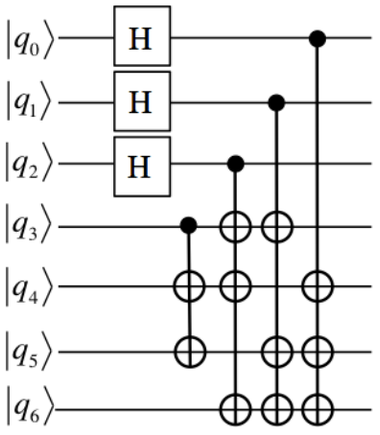
Compilation of quantum circuits: NISQ devices

Transform the circuit to satisfy the target **quantum processor constraints**

```
#qubits definition
qubits 7

h q0
h q1
h q2
cnot q3,q5
cnot q3,q4
cnot q2,q3
cnot q2,q4
cnot q2,q6
cnot q1,q3
cnot q1,q5
cnot q1,q6
cnot q0,q4
cnot q0,q5
cnot q0,q6
```

QASM instructions

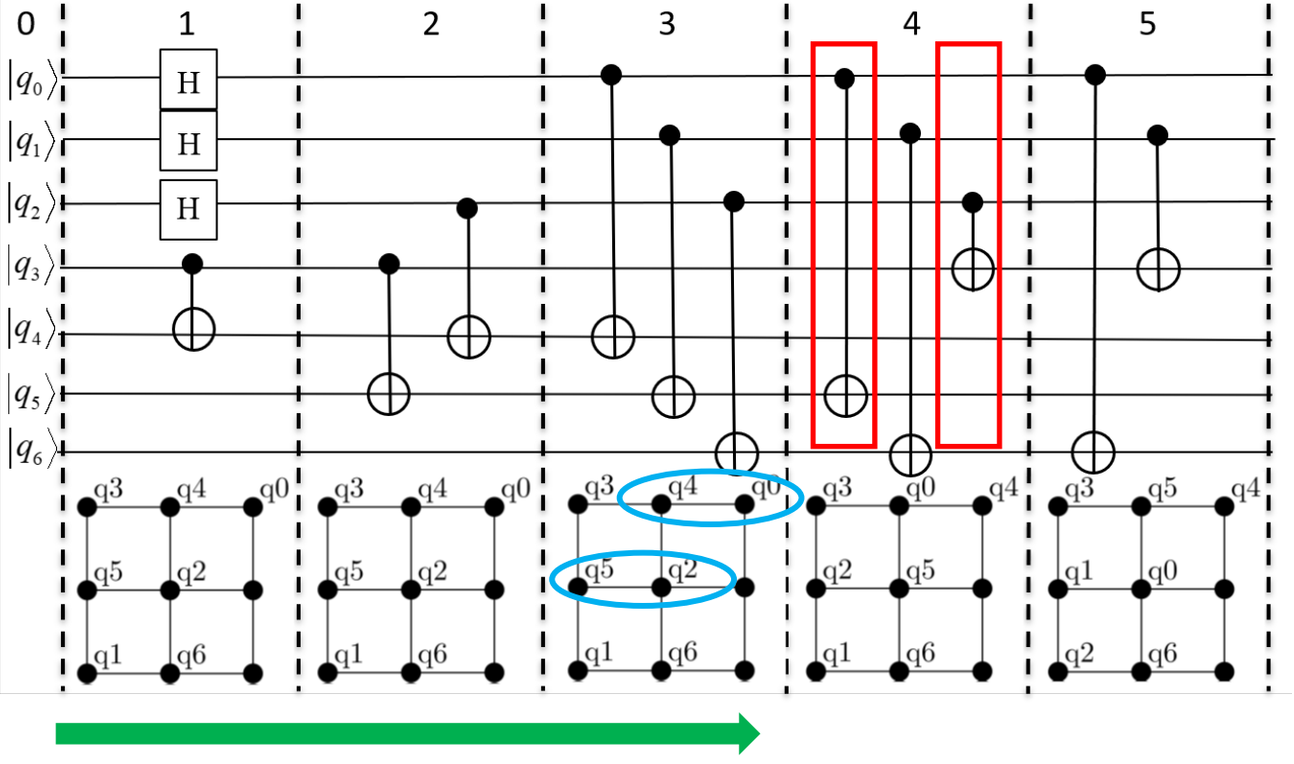


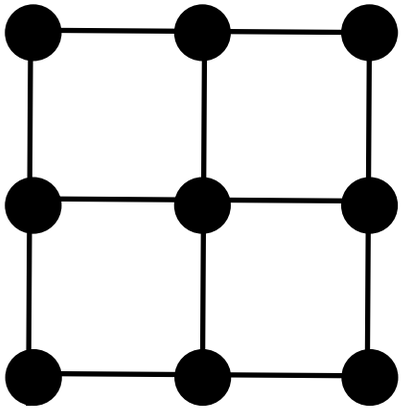
Circuit

Schedule operations to exploit parallelism

{h q0 | h q1 | h q2 | cnot q3,q4}
{cnot q2,q4 | cnot q3,q5}
{cnot q0,q4 | cnot q1,q5 | cnot q2,q6}
{cnot q0,q5 | cnot q1,q6 | cnot q2,q3}
{cnot q0,q6 | cnot q1,q3}

Routing of qubits





Placement of qubits : those that will interact close to each other

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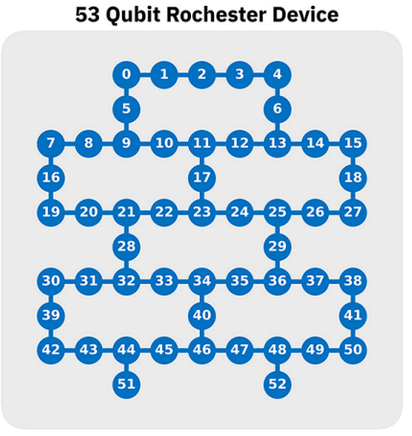
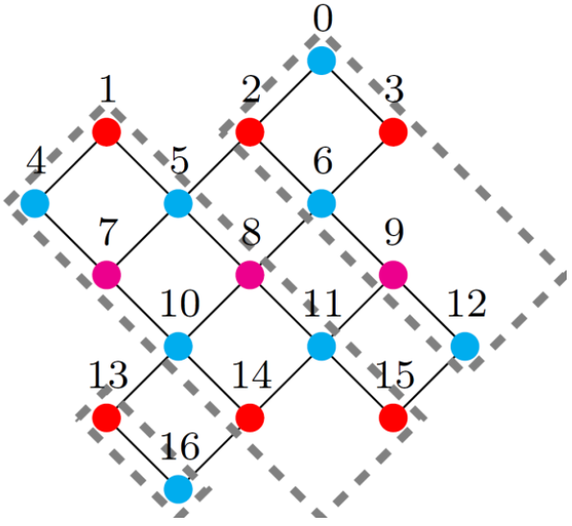
Compilation of quantum circuits: NISQ devices

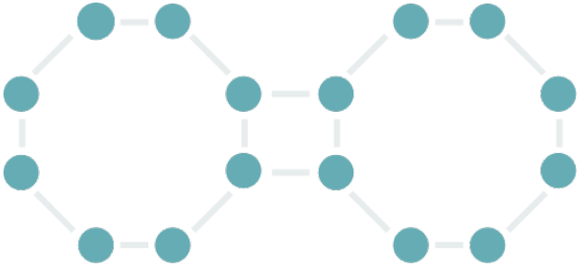
Hardware constraints

- **Elementary gate set:** Single-qubit rotations and CZ
- **Limited connectivity (topology):** Nearest-neighbor interaction on 2D architectures
- **Classical control:** Control electronics are shared among qubits, e.g. three frequencies (red, pink, blue, green) are used for single-qubit gates in Surface-17

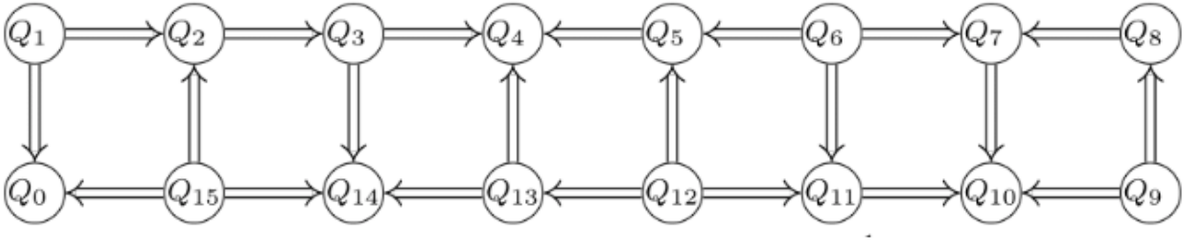


Surface-17
QuTech-Intel





Aspen
Rigetti



IBM QX5

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Compilation of quantum circuits: NISQ devices

The mapping problem is NP-complete constrained optimization problem

Main approach

- To use heuristic search to build the circuit to respect the constraints. The circuit is rebuilt step-by-step. Requires an initial placement of qubits.

    - Satisfiability modulo theory (STM) solvers
    - Greedy randomized search and genetic algorithms

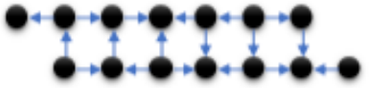
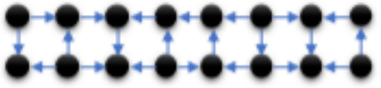
Alternative AI approaches

- Use temporal (AI) planners aided by constraint programming
- Reinforcement learning for qubit routing

Cost function:

- Number of gates – e.g. SWAP gates
- Circuit depth
- Success rate of the algorithm

Compilation of quantum circuits: NISQ devices

Machine	Qubits	2Q Gates	Coherence Time (us)	1Q Error (%)	2Q Error (%)	RO Error (%)	Qubit Topology
IBM Q5 Tenerife	5	6	40	0.2	4.76	6.21	
IBM Q14 Melbourne	14	18	30	1.19	7.95	9.09	
IBM Q16 Rüschlikon	16	22	40	0.22	7.14	4.15	
Rigetti Agave	4	3	15	3.68	10.8	16.37	
Rigetti Aspen1	16	18	20	3.43	8.92	5.56	
Rigetti Aspen3	16	18	20	3.79	5.37	6.65	
UMD Trapped Ion (UMDTI)	5	10	1.5×10^6	0.2	1.00	0.6	

P. Murali, et al. "Full-Stack, Real-System Quantum Computer Studies: Architectural Comparisons and Design Insights." *arXiv preprint arXiv:1905.11349* (2019).

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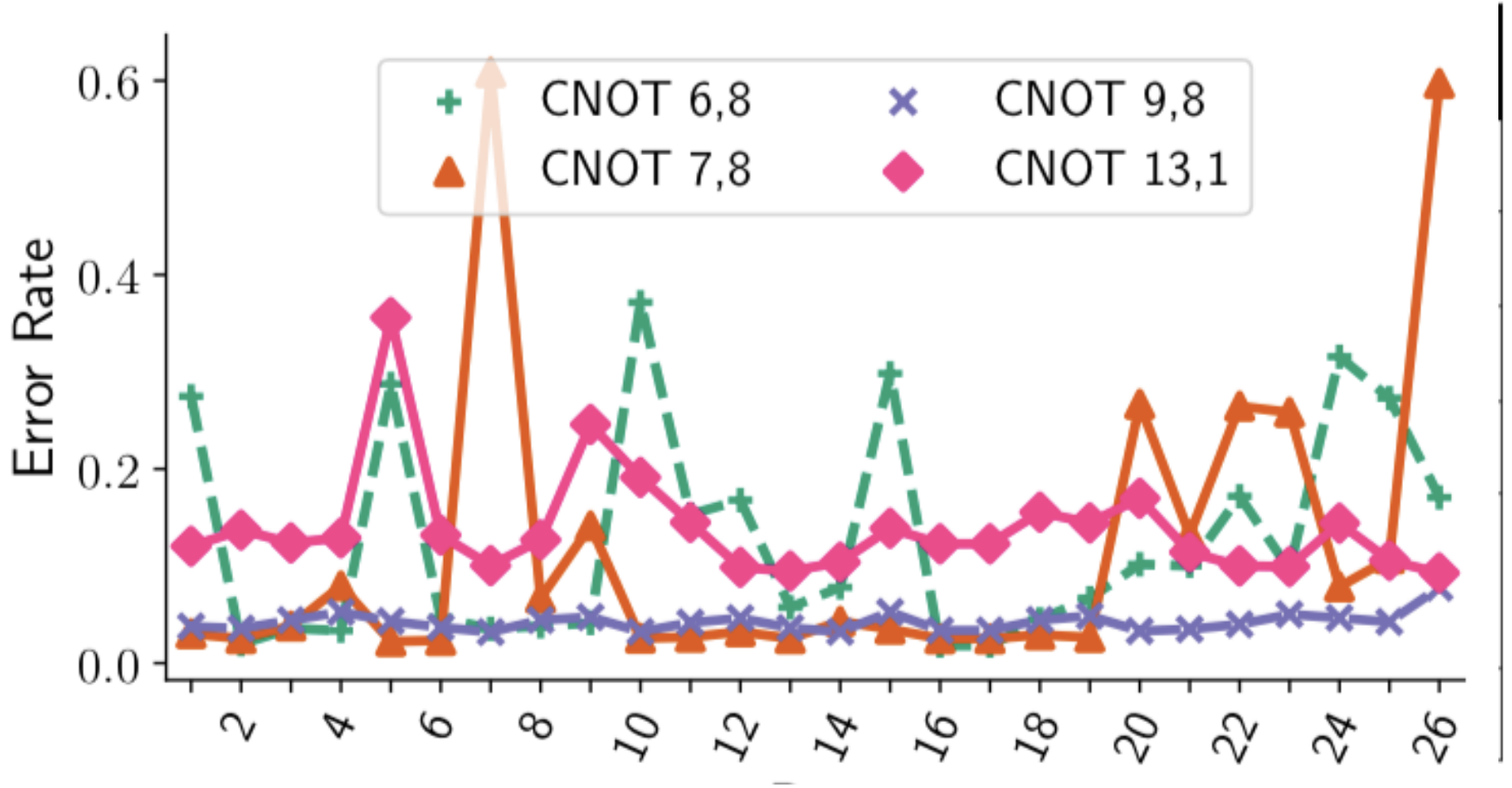
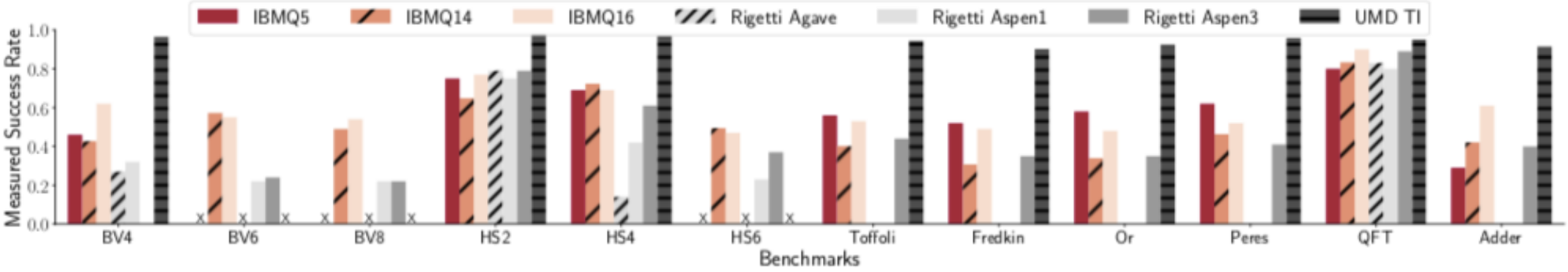
Compilation of quantum circuits: NISQ devices





P. Murali, et al. "Full-Stack, Real-System Quantum Computer Studies: Architectural Comparisons and Design Insights." *arXiv preprint arXiv:1905.11349* (2019).

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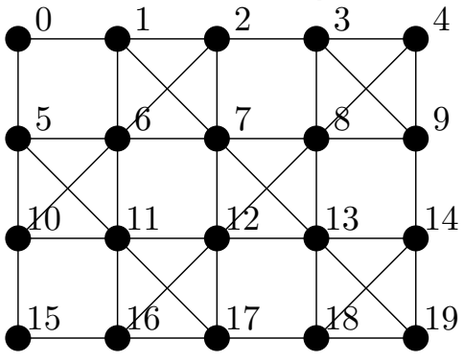
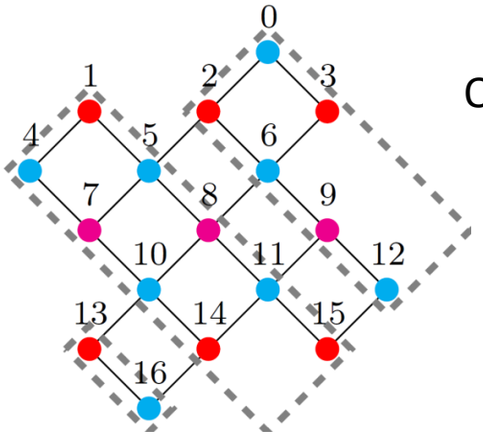
Compilation of quantum circuits: NISQ devices

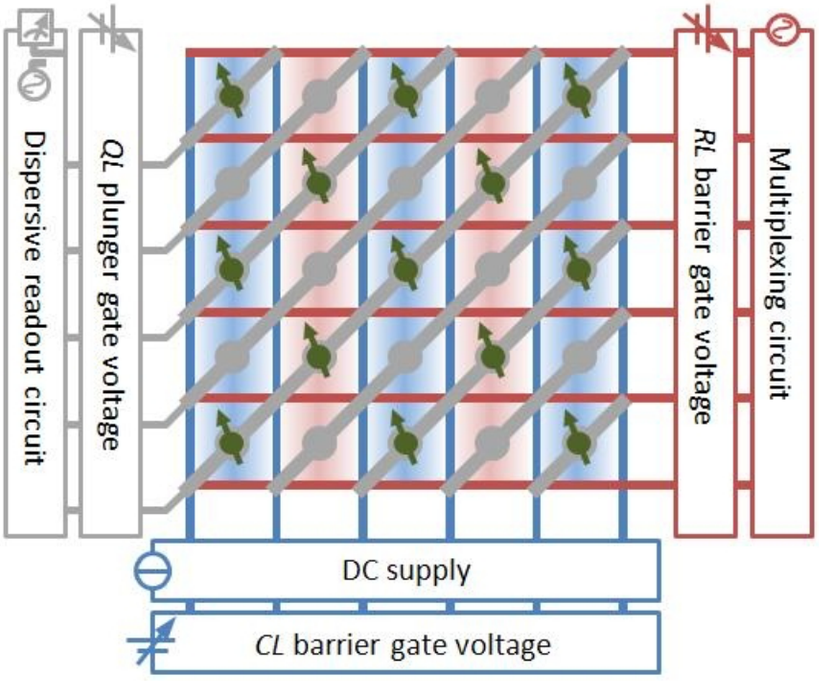
IBM Q Tokyo



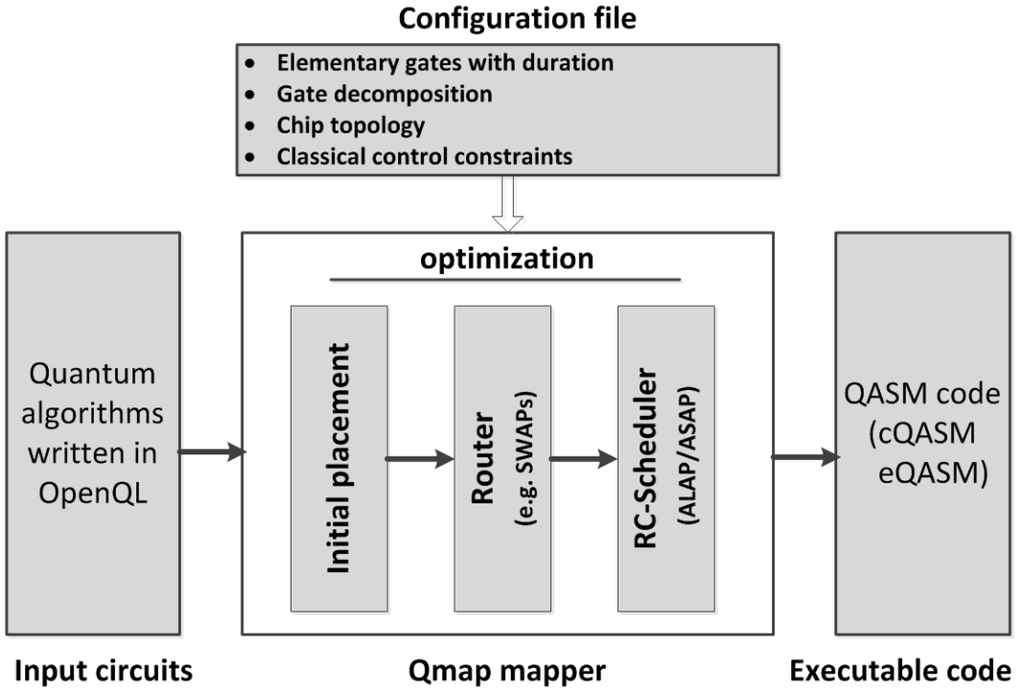


Surface-17
QuTech-Intel

R. Versluis,, et al. "Scalable quantum circuit and control for a superconducting surface code." *PARA.* 2017.



R. Li, et al. "A crossbar network for silicon quantum dot qubits." *Science advances* ,2018.



L. Lao, et al. "Mapping of quantum circuits onto NISQ superconducting processors." *arXiv preprint arXiv:1908.04226*(2019).

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Compilation of quantum circuits: NISQ devices

Summary

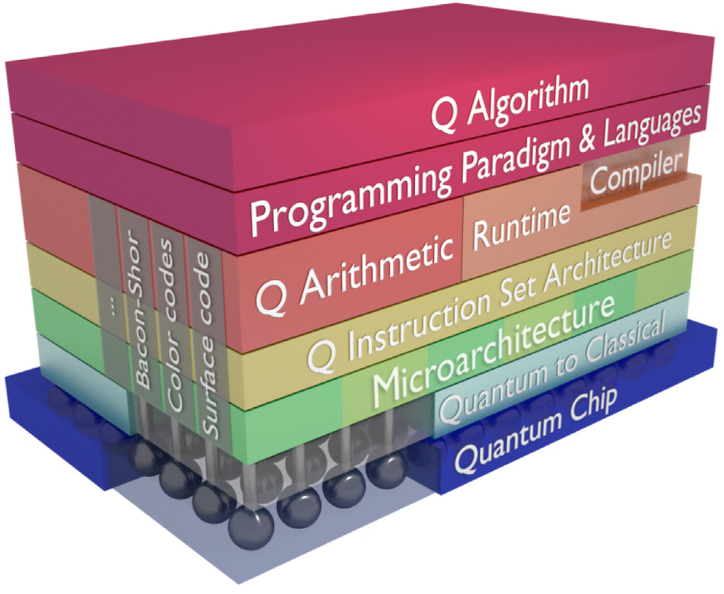
- Optimal mapping strategies depend on both algorithm characteristics and quantum processor constraints
- Technology- specific compiler or general-purpose compiler
- Metrics and cost functions need further research
- So far, bottom-up approach (most of the works focus on superconducting qubits and IBM chips)

Structured DES methodologies for quantum computing architectures: a full-stack vertical co-design framework

Bottom-up approach: Machine-specific SW for NISQ HW
Top-down approach: Application-specific SW for NISQ HW

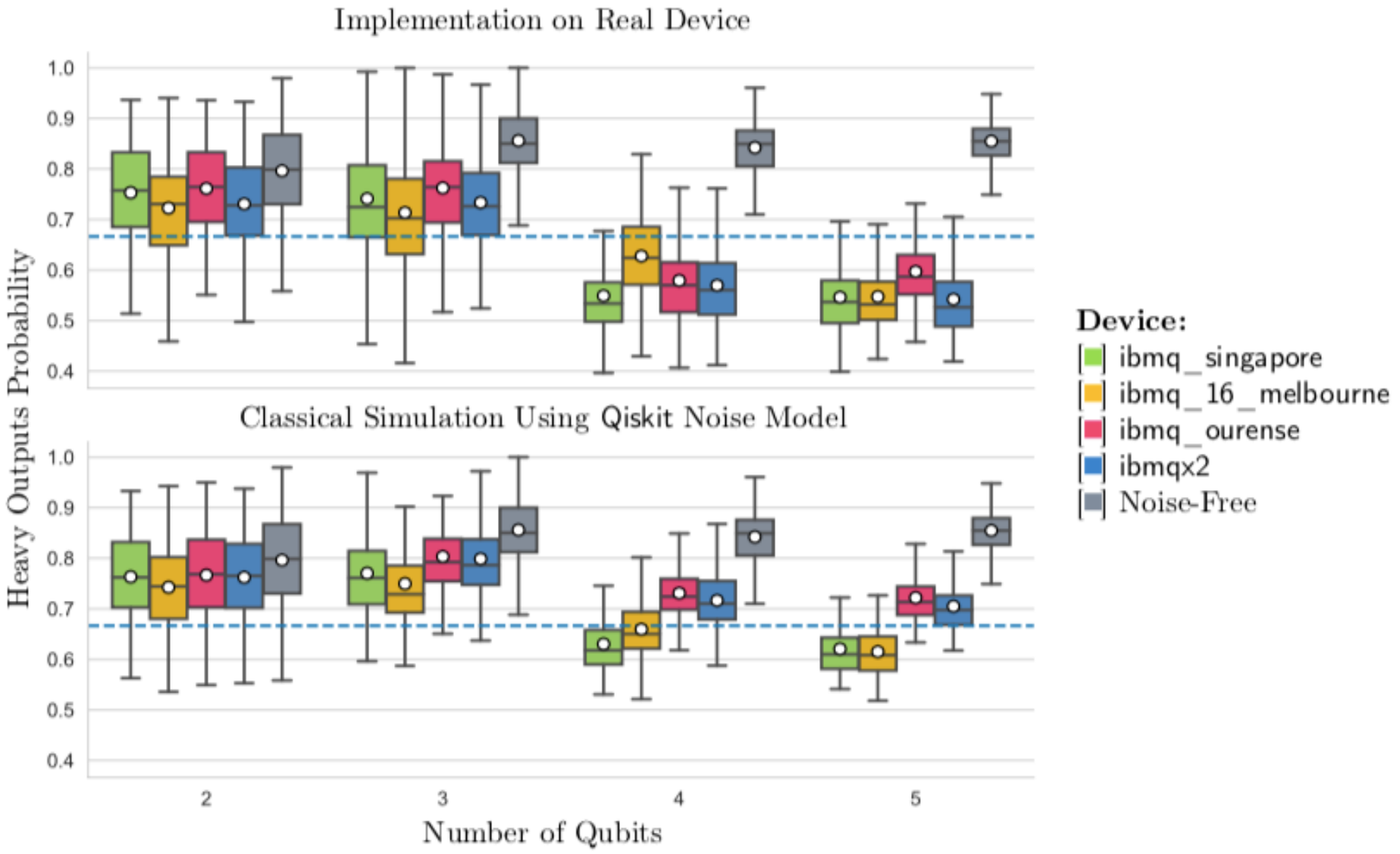
Towards full-stack design space exploration: Top-down and bottom-up

- Optimise for a specific technology and application
- Provide HW design guidelines
- Scalability analysis
- Benchmark quantum systems against different quantum technologies



- Define complete and representative set of benchmarks and overall performance metrics

Benchmarking full-stack quantum computing systems



D. Mills et al., "Application-Motivated, Holistic Benchmarking of a Full Quantum Computing Stack," *arXiv preprint arXiv:2006.01273*, 2020.

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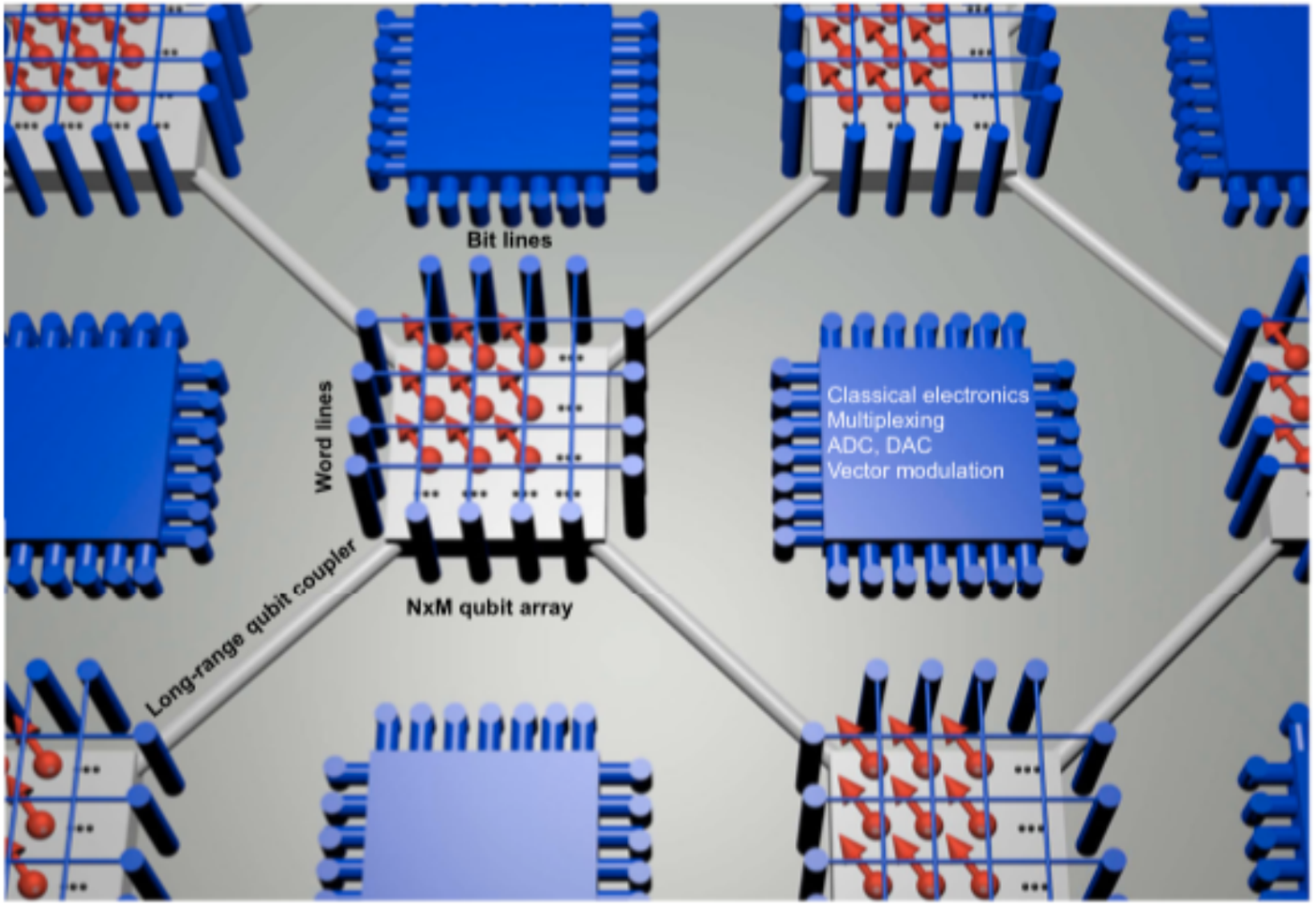
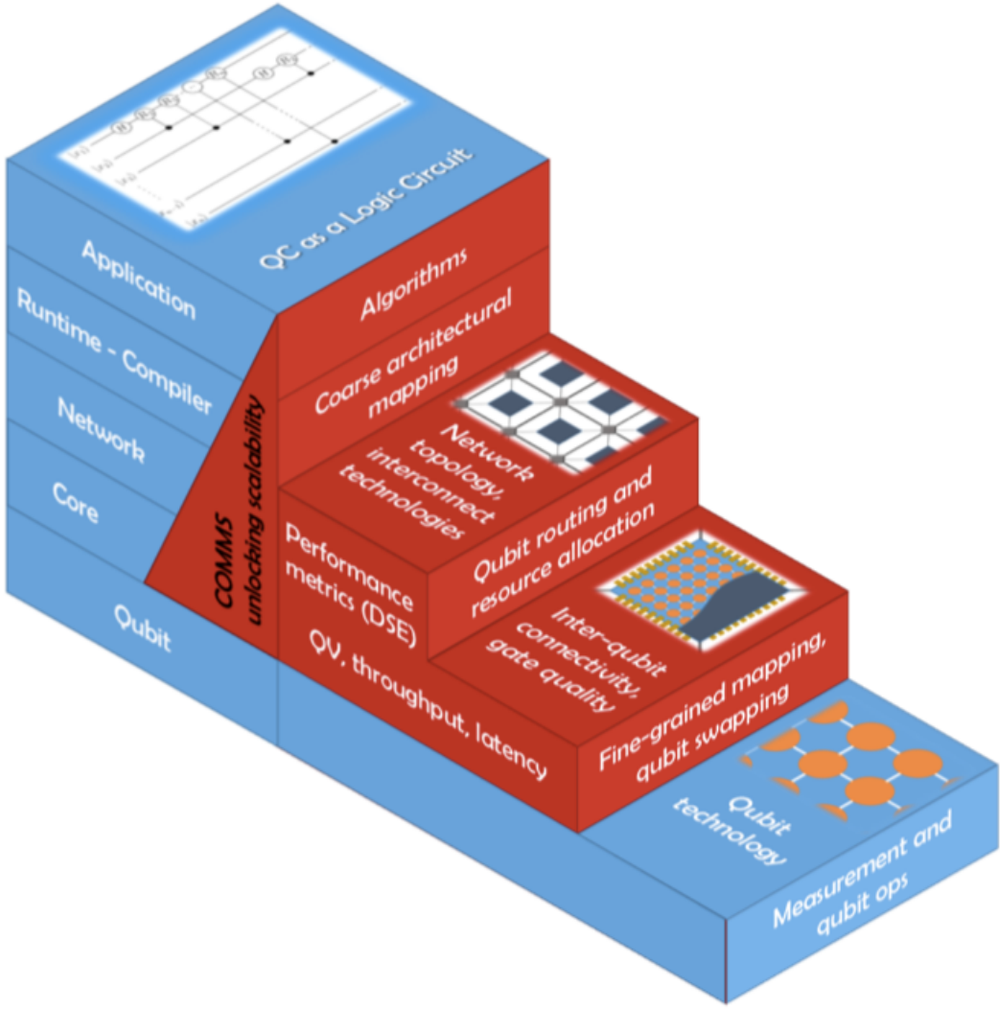
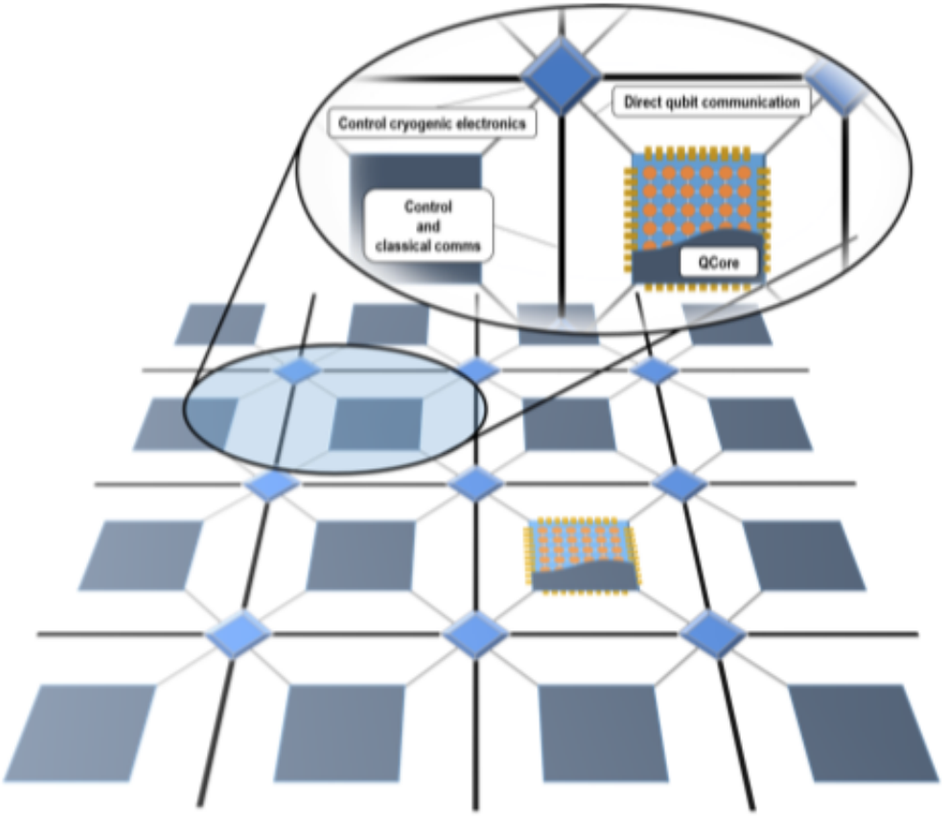
Scalable Distributed (Modular) Architectures



L. Vandersypen et al., “Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent,” npj Quantum Information, 2017.

Scalable Quantum Distributed Architectures: Computation and Communication stacks





S. Rodrigo, S. Abadal, C.G. Almudever and E. Alarcón, "Will Quantum Computers Scale Without Inter-Chip Comms? A Structured Design Exploration to the Monolithic vs Distributed Architectures Quest", in progress (check arxiv soon).

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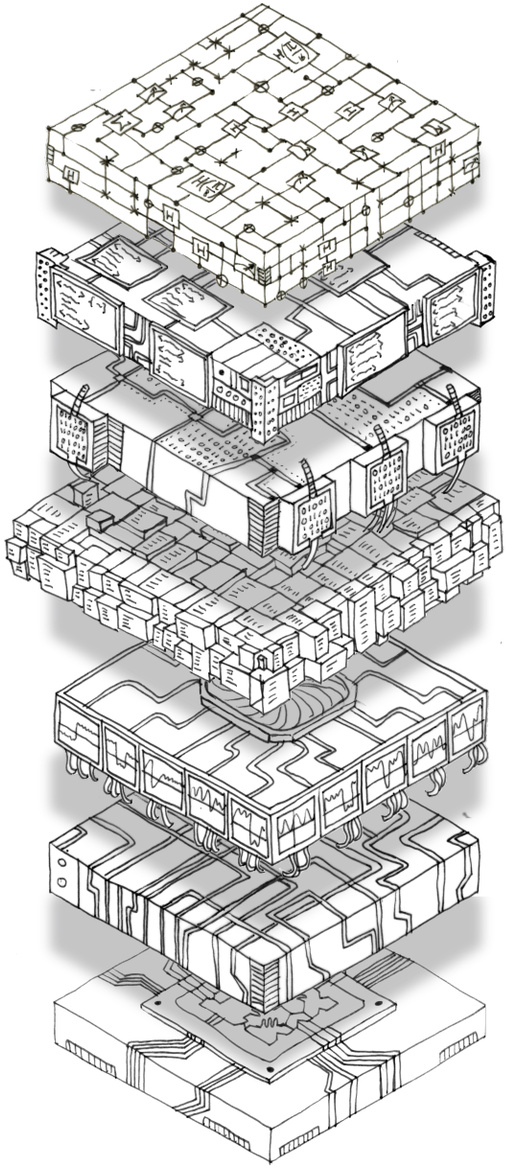
A Quantum Computer Architecture Perspective: Executing Quantum Applications on Real Quantum Processors

Thank you!



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