

OX16PCI954

QUAD UART WITH PCI INTERFACE

EVALUATION BOARD

This document describes the OX16PCI954 evaluation board, how to set its configuration, install drivers and troubleshoot common problems.

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2 **DESCRIPTION**

The development board for OX16PCI954 users provides an environment in which the various modes and features of the OX16PCI954 device can be demonstrated.

It provides a simple means of realising the following products:-

- 8-port serial card (using four internal UARTs and an OX16C954 on a local bus connection)
- 4-port serial / 1 parallel port card (using only functions internal to the OX16PCI954)
- 4-port serial card with pin-assignable Subsystem ID and subsystem Vendor ID
- 32-bit bridge

The specific features available include:-

- Configuration into any of the four device modes available
- Access to the four OX16C950 UARTs (2xRS232, 2xRS422) from a standard 37-way D-type interface
- Use of the 8-bit local bus function to drive an external OX16C954 UART (2xRS232, 2xRS422) from a similar interface
- Use of the parallel port function via a standard 25-way D-type header
- A serial EEPROM socket to provide maximum device configurability
- Use of the internal crystal oscillator, or any frequency via a TTL oscillator socket (switchable). The external OX16C954 can be driven from the TTL module, or directly from the LB_Clk_Out pin of the PCI device.
- Use of isochronous mode feature of the internal UARTs via simple connections
- Test points so that all signals on any bus can be observed easily.

3 BOARD LAYOUT

The layout of the development board is shown in figure 1.

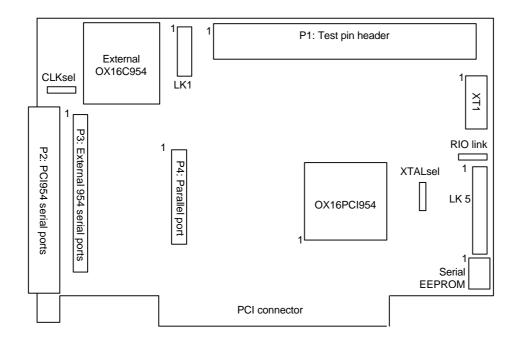


Figure 1: Evaluation board layout

Key

P1:	Test pin header – all non-PCI pins can be accessed here
P2:	37-way 'D' connector for access to PCI UART serial ports
P3:	header for access to external UART serial ports
P4:	header for parallel port
LK1:	DTR/DSR header for RS422 channels
LK5:	configuration header
RIO link:	Connect RI from PCI UART channel 0 or external UART channel 0 to MIO0
XT1:	socket for TTL crystal oscillator
XTALsel:	select internal oscillator or TTL module
CLKsel:	select TTL module or LB_Clk_Out
Serial EEPROM:	socket for serial EEPROM

All links settings are detailed from page 5 onwards. Please note that some boards also have a parallel-port data transceiver (IC13 next to the parallel port header). This should be disabled if the local bus is being used.

4 OPERATION

In any mode the device requires an external clock. Ensure a jumper is fitted to XTALsel, selecting either the crystal or a TTL module which must be fitted to XT1. If the OX16C954 device is being used, a jumper must be fitted to CLKsel, selecting either the TTL module which must be fitted, or the LB_CIk_Out of the 0X16PCI954; this must be enabled by writing to the configuration register.

To use the device as a **Quad UART + 8-bit local bus**, set the mode pins to '00' and insert the OX16C954 device into the socket. Disable the parallel port transceiver. For both the PCI UARTs and the local bus UARTs, channels 0 and 1 interface via RS232 connections, and channels 2 and 3 interface via RS422 connections. The DTR and DSR signals of the RS422 ports are available via the LK1 header – an extra cable is needed if these lines are required. Basic hardware flow control can be achieved without these, however they will be required for DTR/DSR flow control or isochronous mode operation.

Connect the extra 37-way D connector to P3, and if the RS422 channels are required enable them via LK5. The board is now ready for use.

To use the device as a **Quad UART + parallel port**, set the mode pins to '01' and remove the OX16C954 device from the socket. Disable the parallel port transceiver. The UART channels interface as above.

Connect the parallel port header to P4, and if the UART's RS422 channels are required enable them via LK5. The board is now ready for use.

To configure the OX16PCI954 via the **serial EEPROM**, merely insert the EEPROM into its socket. All features of the device can be programmed into the PROM via the OXPROM.EXE utility.

The PCI UART can use the internal crystal oscillator or an external TTL clock source. Select the mode required using the XTALsel link. The external UART can also use the TTL source or the LB_Clk_Out line from the OX16PCI954. Select the mode required using the CLKsel link, and enable/disable the LB_Clk_Out line as appropriate via the local configuration registers. (This can be done with the Microsoft DEBUG utility, or in the serial EEPROM.

To use the Local bus in **Motorola mode**, short the Intel/Motorola# link on the LK5 header. In this mode the default Local bus timing values should be changed in the local configuration registers as follows:-

Read-not-Write De-assertion = 4 Read Data-strobe assertion = 1

- Write data-strobe assertion = 1
- Write data-strobe de-assertion = 3

Also, MIO[8] in the MIO configuration registers should be configured to an inverting input, and MIO[9-11] masked off. An EEPROM configuration file, motorola.dat has been provided for this purpose.

5 DRIVER INSTALLATION

For detailed instructions on how to install the reference drivers, please refer to the application note "Reference Drivers" supplied with this document.

6 CONFIGURATION

The board and device are configured using the configuration header LK5. The pinout is shown in Figure 2. (All links are shown oriented with Figure 1).

	1
••	External FIFOSEL#
	Low power enable
	INTEN#
$\bullet \bullet$	Intel/Motorola# mode
$\bullet \bullet$	RS422 enable
$\bullet \bullet$	TEST
$\bullet \bullet$	MODE1
$\bullet \bullet$	MODE0
$\bullet \bullet$	PCI FIFOSEL

Figure 2: Configuration header LK5

The table below shows the function of each pair of pins

F ns	S lort	C pen
External FIFOSEL#	External FIFOSEL# External UART has 128-deep FIFOs	
LPTBUF#	Parallel port transceiver disabled	Parallel port transceiver enabled
Low power enable Allow driver to shutdown RS23 drivers		RS232 line drivers always enabled
INTEN#	External UART interrupts enabled	External UART interrupts enabled dependent on MCR[3]
Intel/Motorola# mode	Motorola-type local bus	Intel-type local bus
RS422 enable	Enable RS422 line drivers	Disable RS422 line drivers
TEST	Always short	Do not open connection
MODE1	Mode[1] = 1	Mode[1] = 0
MODE0	Mode[0] = 1	Mode[0] = 0
PCI FIFOSEL	PCI UART has 128-deep FIFOs	PCI UART has 16-deep FIFOs

Select the device mode as follows:-

Mode[1:0] = '00' : Quad UARTs & 8-bit local bus Mode[1:0] = '01' : Quad UARTs & parallel port Mode[1:0] = '10' : Quad UARTs & pin-assignable Subsystem ID and Subsystem Vendor ID Mode[1:1] = '11' : 32-bit bridge

7 MISCELLANEOUS LINK SETTINGS

XTALsel: select oscillator for OX16PCI954

TTL oscillator

Select desired oscillator by linking from centre to the pin required.

CLKsel: select oscillator for external UART

TTL module ••• LB_Clk_Out

Select desired oscillator by linking from centre to the pin required

RIO link: connect MIO0 to RI of PCI UART channel 0 or external UART channel 0

PCI UART RI0 • • External UART RI0

Select RI desired by linking centre to that desired. Default = no link. If this is used, MIO[0] should be reconfigured in the local configuration registers otherwise an interrupt on function 0 will be constantly present.

Pinout of RS422 ports:

RS422 supports much higher data transfer rates due to its differential signalling. The RS422 ports are connected as follows on the 9way D-connectors:-

Fin	िgnal
1	TXD-
2	TXD+
3	RTS-
4	RTS+
5	GND
6	RXD-
7	RXD+
8	CTS-
9	CTS+

LK1: The lines provided on the RS422 connectors only allow for CTS/RTS flow control. If DTR/DSR flow control is needed, header LK1 provides access to the extra hardware lines. The pinout is as follows:-

DSR2-	$\bullet \bullet$	DTR2-
DSR2+	$\bullet \bullet$	DTR2+
GND	$\bullet \bullet$	DTR3-
DSR3-	$\bullet \bullet$	DTR3+
DSR3+	$\bullet \bullet$	NC

P1: Test pins

	1 3	2
С		
В		
А		,

	Α	В	С
1	MIO0	MIO1	MIO2
2	MIO3	MIO4	MIO5
3	MIO6	MIO7	LBRST#
4	PE	BUSY	ACK#
5	SLCT	ERR#	LBCS0#
6	LBCS1#	LBCS2#	LBCS3#
7	LBRD#	LBWR#	GND
8	GND	LBCLK	GND
9	SLIN#	INIT#	AFD#
10	STB#	GND	LBDOUT
11	PD0	PD1	PD2
12	PD3	GND	PD4
13	PD5	PD6	PD7
14	MIO8	MIO9	MIO10
15	MIO11	RXD3	RI3
16	DCD3	DSR3	CTS3
17	DTR3	RTS3	GND
18	GND	GND	GND
19	TXD3	TXD2	RTS2
20	DTR2	CTS2	DSR2
21	DCD2	RI2	GND
22	GND	LB_Clk_Out	GND
23	RXD2	RXD1	RI1
24	DCD1	DSR1	CTS1
25	DTR1	RTS1	TXD1
26	TXD0	RTS0	DTR0
27	CTSO	DSR0	DCD0
28	RIO	RXD0	GND
29	GND	FIFOSEL	VCC
30	GND	TEST	VCC
31	GND	MODE1	VCC
32	GND	MODE0	VCC

Pinout of 37-way D-type connector

The following pin description is the same for the PCI internal UARTs and the four ports from the OX16C954 local bus device

37-way D-type pin number	Port number / type	9-way D-type pin number	escription
1	Port 1 / RS232	1	DCD
20	Port 1 / RS232	6	DSR
2	Port 1 / RS232	2	RxD
21	Port 1 / RS232	7	RTS
3	Port 1 / RS232	3	TxD
22	Port 1 / RS232	8	CTS
4	Port 1 / RS232	4	DTR
23	Port 1 / RS232	9	RI
5	Port 1 / RS232	5	GND
24	Port 2 / RS232	1	DCD
6	Port 2 / RS232	6	DSR
25	Port 2 / RS232	2	RxD
7	Port 2 / RS232	7	RTS
26	Port 2 / RS232	3	TxD
8	Port 2 / RS232	8	CTS
27	Port 2 / RS232	4	DTR
9	Port 2 / RS232	9	RI
28	Port 2 / RS232	5	GND
10	Port 3 / RS422	1	TxD-
29	Port 3 / RS422	6	RxD-
11	Port 3 / RS422	2	TxD+
30	Port 3 / RS422	7	RxD+
12	Port 3 / RS422	3	RTS-
31	Port 3 / RS422	8	CTS-
13	Port 3 / RS422	4	RTS+
32	Port 3 / RS422	9	CTS+
14	Port 3 / RS422	5	GND
33	Port 3 / RS422	1	TxD-
15	Port 3 / RS422	6	RxD-
34	Port 3 / RS422	2	TxD+
16	Port 3 / RS422	7	RxD+
35	Port 3 / RS422	3	RTS-
17	Port 3 / RS422	8	CTS-
36	Port 3 / RS422	4	RTS+
18	Port 3 / RS422	9	CTS+
37	Port 3 / RS422	5	GND
19	NC	NC	NC

8 TROUBLESHOOTING COMMON PROBLEMS

Problem: The system doesn't detect the correct devices **Solution:** Make sure the TEST link on LK5 is shorted, and the MODE links are set correctly

Problem: The system detects the ports but a terminal application will not recognise them.

Solution: Ensure that the application supports COM ports other than the four legacy addresses (3f8, 2f8, 3e8, 2e8). If not, use an application that supports all COM devices, such as Quarterdeck Procomm Plus®, or Ericom PowerTerm®.

Problem: Some or all of the ports will not communicate with other devices

Solution: Ensure that the baud rates are correct. The OX16C95x family of UARTs has a very flexible baud rate generator, which can accept differing crystal frequencies, prescalar values etc. The serial port configuration utility in the Windows 9x driver can set baud rate multipliers etc. or completely override an application's baud rate setting.

Solution: Two of the ports on each UART chip have RS422 line drivers. These support higher data transfer rates, but will not interface to RS232 ports. Ensure that the correct ports are being used.

Solution: Ensure that the parallel port transceiver is disabled (link 2 on the LK5 block should be short)

Solution: Ensure that the port has a clock signal, either from the OX16PCI954 oscillator, or from the TTL clock module. This is selected with XTALsel (internal UARTs) and CLKsel (local bus UARTs)

Problem: The parallel port is recognised, but will not communicate with the printer or other device

Solution: Ensure that the parallel port transceiver is enabled if present (link 2 on the LK5 block should be open), also remove the OX16C954 from the PLCC socket

Problem: The local bus will not work in Motorola mode **Solution:** there is a connection missing on the development board. Call Oxford Semiconductor for details

Problem: When the board is installed in a system, it complains of a resource clash.

Solution: PCI devices should be able to share interrupts, however, not all other devices have drivers written to handle this. If another device is using one of the interrupts which is being assigned to the OX16PCI954, there are various things that can be done to work around this problem.

- 1) Move the OX16PCI954 board to a different PCI slot
- 2) Change the settings in your system BIOS to allocate different resources (not all BIOSes have this feature)
- 3) Use the serial EEPROM to only allocate one interrupt to the two OX16PCI954 functions
- 4) Disable any non-critical device that is using the same interrupt for instance USB controllers can often not share resources adequately.

Problem: The PC will not turn off with the OX16PCI954 installed.

Solution: Apply a PME# pin isolator as recommended in the application notes. Newer demonstration boards have this modification applied.

9 REFERENCE DRIVER / UTILITY DISK

The disk supplied contains a reference Windows 9x driver, a reference Windows 2000 driver, and reference drivers for Windows NT4. It also contains related utilities and documentation.

The contents are listed below:-

l	oxpar.inf oxpci.inf oxpci2.inf oxser.inf oxmep.sys oxmf.vxd/sys oxmfuf.sys oxpr.vxd oxser.vxd/sys oxpp.vxd oxser.vxd/sys oxppui.dll oxserui.dll	
\oxprom	oxprom.exe oxeeprom.sys .dat files	 Serial EEPROM programming utility needed by oxprom.exe example EEPROM configuration files
\utils	readuart.exe poke.exe .vxd files	 dump UART registers from within Win9x. memory access utility needed by above utilities
\doc		 this file advanced baud rate configuration in Windows 2000 details on customising drivers df - driver installation and use
\NT4_Parallel	Install_Parallel.exe oxpar.inf oxpar.sys licence.txt	
\NT4_Serial	Install_Serial.exe oxser.inf oxser.sys licence.txt	 install program for Windows NT4 serial port driver installation script port driver licence agreement

10 NOTES

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11 Appendix A: Reference PCB Issue B differences

In line with its policy of continuing development Oxford Semiconductor has revised and re-issued the PCI 954 Reference PCB, providing a board which is both easier to use and more reliable. The few changes visible to the end user are documented here.

The External OX16C954, labelled IC1 has been rotated 90° clockwise. Pin 1, marked by a dimple and a bevelled edge on the IC, should be facing the right of the board, away from the serial connectors.

LK5 has been renamed JP3, but remains in the same position, and maintains the same functionality, with these exceptions:

The parallel port has no transceiver buffers, and hence LPTBUF# is not used.

The RS232 line drivers are permanently enabled, so Low Power Enable is no longer connected.

The RS422 line drivers also permanently enabled, so RS422 Enable is no longer required.

TEST has been permanently shorted on the PCB, and no jumper is required on this pin.

For compatibility these jumpers are physically present, but have no electrical function.

P4: the Parallel port, has been renamed JP7, but remains in the same place with the same connectivity and function.

P3: External 954 serial ports has been renamed JP1, but again retains the same position and connectivity.

P1: Test Pin Header has been renamed JDH1, with the pinout remaining the same.

XT1 is renamed to JS1.

Serial EEPROM has been renamed to IC7

12 CONTACT INFORMATION

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