BACKPLANE SIGNAL TABLE

Pin #	ROW a	ROW b	ROW c
1	SS14	UTL-E-RXD	SS15
2	SS12	UTL-E-TXD	SS13
3	SS10	TIM-A-CDAC	SS11
4	SS08	UTLRST	SS09
5	SS06	*USER	SS07
6	SS04	*USER	SS05
7	SS02	*USER	SS03
8	SS00	*USER	SS01
9	GND	*USER	GND
10	SCLK	*HVEN	AD00
11	GND	*USER	AD01
12	BUS-CLK	TIM-A-SCK	AD02
13	TIM-D-AUX	TIM-A-STD	AD03
14	TIM-ADA0	TIM-ADA1	AD04
15	GND	TIM-ADA2	AD05
16	TIM-ADA3	TIM-ADA4	AD06
17	GND	TIM-ADSTR	AD07
18	TIM-U-WDT	UTL-T-TXD	AD08
19	GND	UTL-T-RXD	AD09
20	EXT-U-IRQ	GND	AD10
21	*LVEN	TIM-U-SCK	AD11
22	*PWRST	TIM-U-STD	AD12
23	UTL-T-SCK	GND	AD13
24	UTL-T-STD	UTL-T-IRQ	AD14
25	STATUS0	EXT-T-IRQ	AD15
26	STATUS1	PWROK	AD16
27	STATUS2	TIM-A-WRSS	AD17
28	STATUS3	TIM-A-ENCK	
29	TIM-V-AUX1	LVEN	TIM-U-RST
30	TIM-LATCH0		EXT-T-RST
31	-16V	+32V	+16V
32	+5 VDC	+5 VDC	+5 VDC

* The VME backplane does not bus these signals to all slots.

EXPLANATION OF BACKPLANE SIGNAL NAMES

AD00 -> AD17	Analog-to-Digital converter data. Least significant bit is AD00.
BUS-CLK	System clock generated by the timing board for use by other boards.
EXT-T-IRQ	Generated by an external source to request a timing board interrupt on IRQB*.
EXT-T-RST	External signal to reset the timing board.
EXT-U-IRQ	External signal to request interrupt service from the utility board.
HVEN	Generated by the utility board to turn on the power control board's high voltage switches.
LVEN	Generated by the utility board to turn on the power control board's low voltage switches.
PWROK	Generated by the power control board to signal that the power supply voltages are within limits.
PWRST	Reset the power control board, and turn off the low and high voltages.
SCLK	Serial clock used for asynchronous serial interface in synchronous mode.
SS00 -> SS15	Switch state bits generated by the timing board to control clock driver and video processor analog switches. Bits 0-11 are used for switch states, and bits 12-15 are used for board select.
STATUS0 -> STATUS3	Four programmable status lines running from the timing board DSP general purpose I/O pins to the backplane for general use.
TIM-ADA0 -> TIM-ADA4	Address bits generated by the timing board to select the A/D converter to be read. A total of 32 A/Ds can be read.
TIM-ADSTR	Address strobe signal generated by the timing board to cause A/D values to be written to the lines AD0-AD17 by the video board.
TIM-A-SCK	Synchronous serial clock from the timing board to analog boards.
TIM-A-STD	Synchronous serial data from the timing board to analog boards.
TIM-A-CDAC	Clear all the digital contents of the analog board DACs.
TIM-A-ENCK	Enable the outputs of all the clock drivers and DC bias supplies on the analog boards.
TIM-A-WRSS	The switch states SS0-15 are valid when this signal goes high.
TIM-D-AUX	Timing to clock driver board uncommitted communication line.
TIM-LATCH0	Uncommitted latched signal output from the timing board.
TIM-U-RST	Generated by the timing board to reset the utility board.
TIM-U-SCK	Timing to utility board synchronous clock.
TIM-U-STD	Timing to utility board synchronous data.
TIM-U-WDT	Generated by the timing board to signal to the utility board watchdog circuit that the timing board is alive.
TIM-V-AUX1	Timing to video processor board uncommitted line.
UTL-E-RXD	Utility board to external asynchronous receive data.
UTL-E-TXD	Utility board to external asynchronous transmit data.
UTLRST	Reset the utility board.
UTL-T-IRQ	Generated by the utility board to request a timing board interrupt.

UTL-T-RXD	Utility to timing board asynchronous serial received data.
UTL-T-TXD	Utility to timing board asynchronous serial transmitted data.
UTL-T-SCK	Utility to timing board synchronous clock.
UTL-T-STD	Utility to timing board synchronous transmitted data.

Resets, interrupts, and general system support -

EXT-T-IRQ	EXT-T-RST	EXT-U-IRQ	UTLRST
TIM-U-RST	UTL-T-IRQ	BUS-CLK	TIM-U-WDT

STATUS0 -> STATUS3

Serial communication -

TIM-U-SCK	TIM-U-STD	UTL-T-SCK	UTL-T-STD
TIM-A-SCK	TIM-A-STD	SCLK	
UTL-T-RXD	UTL-T-TXD	UTL-E-RXD	UTL-E-TXD

Power control board functions -

LVEN	HVEN	PWRST	PWROK

Controlling video processor and clock driver boards -

TIM-A-CDAC	TIM-A-ENCK	TIM-D-AUX	TIM-V-AUX1
TIM-ADSTR	TIM-ADA0 -> TIM-ADA4	AD00 -> AD17	
TIM-A-WRSS	SS00 -> SS15		

A high voltage on these lines indicates the following signals are true -

TIM-A-ENCK	PWROK	PWRST	TIM-ADSTR
AD00->AD17	TIM-ADA0 -> TIM-ADA4	SS00 -> SS15	

A low voltage on these lines indicates the following signals are true -

EXT-T-IRQ	UTL-T-IRQ	EXT-U-IRQ	TIM-A-CDAC
TIM-U-RST	UTLRST	EXT-T-RST	

The following signals are clocks or strobes. Data is valid on the high going edge of strobe signals.

BUS-CLK	LVEN	HVEN	SCLK
TIM-A-WRSS	TIM-U-WDT		

Intra Board Communication

A typical system will have a total of four processors that need to communicate with each other - the host computer, the VME or SBus host computer interface board, the timing boards and the utility board. The VMEbus interface has a DSP, while the SBus interface board has a special purpose chip made by LSI Logic to execute direct memory access cycles on the SBus, called the DMA+ chip. The timing and utility boards have DSPs. The boards communicate along a linear path, as shown in Fig.

1-2, wherein a command sent from the host computer to the utility board must pass through the

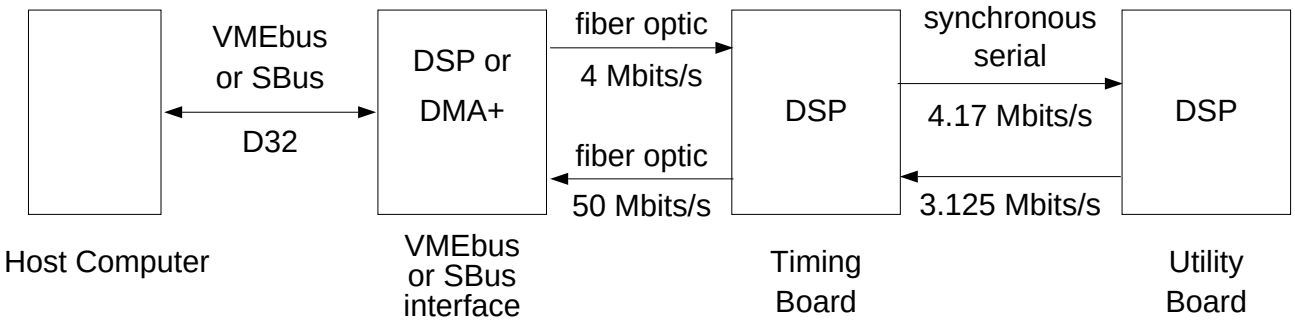

FIG. 2-1: Processor block diagram and communication path

computer interface and timing board -

A communications protocol has been implemented in the DSP code that recognizes that three types of data exist - commands, replies, and image data. Commands and replies are multi-word, short strings that are passed between any of the four components of the system, whereas image data can only be passed from the timing board through the interface and on to the host computer. Commands and replies always contain a header in the first word, formatted according to:

Source byte, destination byte, number of words in command

This is a three byte word, which fits nicely into the 24-bit data word length of the DSP, and source and destination designations are assigned to each of the four processors as follows:

0	Host computer
1	VME interface board
2	Timing board
3	Utility board

The number of words in the string can be from two to seven, and the header is counted as one word. Command and reply strings contain three byte ASCII strings, all upper case, in the second word. Some commands are followed by one or more numbers whose meaning depends on the command. Replies always contain two words total, the header and the reply. For example, the command for the host computer to write a NOP instruction to the Utility board P: memory in the $78'th location is:

$000304 'WRM' $100078 $000000

The utility board will respond to the host computer with a reply:

$030002 'DON',

meaning that the indicated command was executed satisfactorily. The $1 in the most significant nibble

of the address field of the WRM instruction is an encoding scheme to indicate the P: (program memory) is to be updated; X:, Y: and ROM data memory can also be accessed.

A hiearchical philosophy has been adopted in partitioning which boards perform which time critical tasks. The most time critical tasks of CCD readout timing and voltage control are performed by the timing board which operates on a time scale of order one microsec. Similarly, the VME or SBus interface board performs time critical tasks limited to data handling on a microsec time scale. The utility board is next in the hierarchy, performing tasks on a time scale of order one millisec. Non-time critical tasks are performed by the host computer. Paralleling this hierarchy, the microsec time scale boards are capable of only limited error checking and reporting and rely on other system components to manage them. The utility board performs modest error checking and reporting, and initiates timing and VME interface board operations. Finally, the host computer performs extensive error checking and reporting on a non-real-time basis, and directs the utility board to manage time critical operations. As an illustration, the sequence of commands needed to execute a normal timed and shuttered exposure with a VMEbus interface board is:

Host writes exposure time to utility	$000304 ’WRM’ $400018 time
Host writes # of columns to timing	$000204 ’WRM’ $400001 #cols
Host writes # of rows to timing	$000204 ’WRM’ $400002 #rows
Host writes number of pixels to VME	$000104 ’WRM’ $200007 npxls
Host sends start exposure command to Utility	$000302 ’SEX’
Utility sends clear CCD to timing	$030202 ’CLR’
When done, timing send done clear to utility	$020302 ’DON’
Utility opens shutter, starts exposure timer	internal utility board operations
When timer elapses, utility closes shutter, sends start readout command to VME interface	$030102 ’RDC’
Utility send start readout command to timing	$030202 ’RDC’
VME sends done reply to host when readout complete	$010002 ’DON’

The timing board sends image data to the VME interface, which writes it first to on-board buffer memory then to the VMEbus. Similarly, the SBus interface board writes data first to on-board FIFO memory, then to medium-sized system buffers, then to the final large image in user memory space. When npxls have been sent the timing board re-enters either the idle mode or the stop mode depending on whether a ’IDL’ or a ’STP’ command was last issued, and the VME interface enters command interpreting mode.

During readout the VME and SBus interface boards interprets all data coming from the timing board over the fast fiber optic data link as being image data. Both the interface board and the timing board are still looking for commands to allow the host computer to abort the readout in progress if needed. Proper management of the readout parameters is assumed by the host computer, but any task requiring time critical service is initiated by one of the DSP boards.

An initialization procedure is needed after system reset. Because the procedure is not time critical and requires a modest degree of checking to insure that it is completed successfully, it is performed by the host computer:

Test system:	$000103 'TDL' number	reply:	$010002 number
	$000203 'TDL' number	reply:	$020002 number
	$000303 'TDL' number	reply:	$030002 number
Load VME program	$000103 'LDA' 2	reply:	$010002 'DON'
Load timing program:	$000203 'LDA' 2	reply:	$020002 'DON'
Load utility program:	$000303 'LDA' 0	reply:	$030002 'DON'
Turn on analog power:	$000302 'PON'	reply	$030002 'DON'

The commands will reply with 'DON' after completing command execution, if successful. Further system checks after this initialization procedure completes can be made by reading the values of the analog voltages from the utility board Y: data memory table with the 'RDM' command, and performing additional 'TDL' tests after full system initialization.

Bus communication - writing switch states and reading image data

To control and read out detector arrays the timing board generates digital signals that are bussed over the backplane to one or more clock driver boards and one or more video processor boards. On the clock driver board these signals are connected to analog switches that select high or low voltages that are input to op amps that connect to the clock lines of the array. On the video processor board some of these signal connect to analog switches performing the signal processing, and others to the A/D converter to issue a start conversion pulse and to a latches to store the A/D data. These timing signals are generated by having the timing board write from internal memory to latches on the timing board that drive the lines SS0 to SS15. These are" switch state" signals, with SS0-11 controlling the switch states and SS12-15 used as board select so multiple clock driver and video processing boards can be used in a system. There is a strobe signal TIM-A-WRSS that undergoes a low-to-high transition when the data lines SS0-15 are valid. Careful attention has been paid to provide reliable operation with a large and variable number of boards in the system by having the signals SS0-15 valid for the entire 40 nanosec instruction cycle, by using high current bus driver (from the TI ABT series), by placing the TIM-A-WRSS strobe signal at the center of the time that SS0-15 are valid, and by keeping the receiver latching circuits on the clock driver and video processor boards close to the backplane connector to minimize signal rise times. Placing more boards in the system increases the rise time of TIM-A-WRSS and SS0-15 due to increased inductive loading by the signal traces of the added boards. A measurement with 3 boards installed was extrapolated to estimate that the increased delay time will be 10 nanosec with 20 board installed, well within the reliable operating range of 40 nanosec.

To write a number to update the switch states one simply writes the desired number to the memory location X:$FF80, as follows -

```
MOVE      #$ddbsss,A    ; Write switch state sss to board #b with delay dd
MOVE      A,X:$FF80     ; Write this number to the WRSS memory mapped location
```

The bits are encoded as follows -

D16-D23	dd	Delay execution of the next instruction by the following If D23 = 0 then delay by D16-D23 steps of 20 nanosec, plus 80 nanosec If D23 = 1 then delay by D16-D23 steps of 160 nanosec, plus 80 nanosec
D12-D15	b	Board select number, which should match the "SWITCH" jumper setting of either a clock driver or video board
D0-D11	sss	Switch state bits

Two modes of reading image data from the video processor to the timing board are implemented - through the DSP and through a PAL. The DSP can simply read the A/D counts from any one of 32 A/D converters in the system and write it to the fiber optic transmitter with the instruction

```
MOVE    Y:$FFA1,A           ; Read A/D #1 into accumulator
MOVE    A,Y:$FFC0           ; Write accumulator to fiber optic transmitter
```

The A/Ds are memory mapped over the range of Y:$FFA0 to $FFBF. Each of these instructions executes in one DSP instruction time plus one wait state, or 120 nanosec for the two instructions.

An alternative method of reading the A/D counts is to utilize a PAL circuit on the timing board that generates the addresses of the A/Ds to be read from a starting value to an ending value, each of which can be from 0 to 31. The circuit passes the A/D values to the serial transmitter as well, so the DSP only needs to initialize the circuit. This is done by having the DSP write as follows, where the notation % indicates that the word is written in bit, rather than nibble, fashion -

```
MOVE    #%ddddddddd1111xxeeeeebbbbb,A       ; Read A/D numbers 0 to 4
MOVE    A,X:$FF80                           ; Write this number to the PAL
```

The address X:$FF80 is the same one used to write switch states allowing this instruction to be placed in a clocking waveform for minimum overhead. The bits of the data word are encoded as follows -

D16-D23	ddddddddd	Delay, normally not used here
D12-D15	1111	Must be set to $F for this circuit to execute
D10-D11	xx	Not used
D5-D9	eeeee	Ending A/D number
D0-D4	bbbb	Beginning A/D number

For example, MOVE #$00F060,A will read and transmit the A/D values from a quadrant readout system, that is. A/Ds 0 to 3. The beginning and ending numbers can be equal, can range over 0 to 31, but the ending number must be greater than or equal to the beginning number.

Writing to Digital-to-Analog Converters (DACs)

There are DACs on the clock driver board that set the high and low voltages between which the clock switch, and on the video processor board for setting DC bias voltages for the detector arrays and offset voltages within the video processor. The DACs are loaded with digital numbers that are generated by the synchronous serial interface (SSI) circuit of the timing board DSP and transmitted to each DAC by a serial data stream that is decoded by PALs (Programmable Array Logic) on each board. The serial data is sent in 24-bit words, most significant bit first, at a speed of 4.17 Mbits/sec. The 24-bit data word is decoded by the clock driver and video processor boards as follows -

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B3	B2	B1	B0	D3	D2	D1	D0	A0	A1	M1	M0	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

Board Number DAC select

Address of one of 4 DACs in each package

DAC voltage, video processor gain or MUX select

Mode - DAC, gain or MUX select

Fig. 2-2: Bit assignment of serial word trasnsmitted to clock driver and video processor boards.

B3 - B0 Selects the board number that is to be written to. The clock driver and video processor boards have four jumpers headers labeled "DAC address" that need to match the bits in the serial word for the board to accept it. The jumpers are installed to set the bit to zero. Up to 32 clock driver and 32 video processor boards can be addressed in a system.

D3 - D0 Selects the DAC package number to be written to. There are twelve DACs on the clock driver board that are selected by numbers D = 0 to 11, and four DACs on the video processor that are selected by numbers D = 12 to 15. Note that clock drivers and video processor boards can have the same board select number. The Mode bits below must be zero (M0=M1=0)to write to a DAC.

If D2 = D3 = 0 then the V bits will set the MUX address.

If D2 = D3 = 1 then the V bits set the video processor gain.

A0 - A1 There are four DAC circuits in each package, and these two bits simply select which of the four is to be written to.

M0 - M1 Mode bits to select between DAC writes, gain select on video processors and output multiplexer (MUX) select on the clock driver board.

M0 = M1 = 0 to write to a DAC

M0 = M1 = 1 to select a gain or a MUX according to bits D2 and D3.

V0 - V11 The 12-bit digital number written to the DACs to select its output voltage, if writing to a DAC. If the video processing gain is selected then V0 to V3 sets the gain of channel 0 and V4 to V7 of channel #1. If the MUX is selected then they select which of 24 clock driver circuits are connected to the diagnostic connector for examination with an oscilloscope.

Resetting DSPs

A facility exists for resetting the DSPs in a variety of ways. Restting DSP is accomplished simply be bringing its REST* pin low, which causes the DSP on the timing board to read the initializing boot code from on board ROM and the DSP on the utility board to start executing ROM code directly. After a reset the DSP executes the boot code, but the application code is lost by the reset . Several mechanisms exist for the timing board DSP to reset, as follows -

(1) Power-on: A power monitor circuit asserts the reset line several hundred milliseconds after the +5V power Vcc is applied.

(2) Host fiber optic command: If the bit pattern $53xxxxxx is sent by the host computer the serial reciever PAL will issue a DSP reset. This may be useful to remotely resetting the DSP in cases where it is no longer executing commands correctly.

(3) DSP software command: The command 'RST' will cause the DSP to enter the reset state.

(4) Power control board reset switch depression: The reset switch on the power control board can be pressed to generate a low signal on EXT-T-RST which will get passed over the backplane to cause the timing board to reset.

(5) Power supply reset switch depression: The large black pushbutton on the power supply is passed on the power supply cable to the power control board to reset via the EXT-T-RST signal.

Whenever the timing board is reset it will execute a short routine that asserts the TIM-U-RST line that is passed over the backplane to the utility board to reset it. The utility board will be reset by its own power-on circuit, by pressing its own reset switch, by its own watchdog timer circuit (it enabled) or by this timing board signal.

Maximum number of clock driver and video processor boards

There are maximum numbers of both clock driver and video processor boards that can be installed in the system, as determined by logical addressing limits. There is a maximum of 21 boards total that can be installed in a VME backplane, which is just the maximum number of slots in the VMEbus specification. There are other limits imposed by controller size and power dissipation, but this section deals only with the logical addressing limits.

The logical addressing limit for the number of A/Ds in a system is set by the number of signals TIM-ADADR# which are used to address the desired A/D value. TIM-ADADR runs from 0 to 4, so a maximum of 32 A/Ds can be put in a system, or 16 dual readout video processor boards.

Similar, but more complex, limits are set by the number of switch state and DAC board address bits, as follows. There are four address bits (D12-D15) encoded in the switch state word, but one of these ($F) is reserved for the series transmit (SXMIT) function, so fifteen board addresses are available. Each clock driver board has two board addresses, one accessing the bottom 12 clock drivers, and one accessing the top 12 clock drivers. Therefore, 15 clock driver half boards, or 7.5 clock driver full boards, may be separately accessed with different timing instructions. The switch state circuits are designed so that several clock driver boards can be jumpered to the same switch address so they have

the same timing. This is useful in mosaic applications where several detector arrays have the same geometry and the timing needs to be done strictly in parallel for all the arrays in the mosaic.There is no limit for the number of clock drivers with the same board address. Similar considerations apply to the number of video processing boards, though only one switch address is used per board. Because the clock driver and video processor boards utilize the same switch state address field the number of separately addressed video processor boards plus clock driver half boards is 15.

The serial transmitter word that is sent to all the boards to write numbers into the DACs contains a four bit board number address field, and is used for both clock driver and video processing boards. Each DAC board address writes to all the DACs on an addressed clock driver or video processing board, not two addresses per board for the timing data. Also, the board addresses are set up differently for clock driver and video processing boards, so a total of 16 clock driver and 16 video processing boards may be installed in a system. At 24 clocks per clock driver board this works out to a maximum of 384 clocks per system and 32 A/D converters.

To summarize -

Max. number of video processing boards	16
Max. number of clock driver boards	16
Max. number of differently timed video processor boards plus clock driver half boards	15

Fiber Optics Serial Protocol

Required care with fiber optic connectors

Use plastic connectors on fiber optics cables

Use bayonet couplers

Be careful

Compatibility with Gen I components

Utility board is fully compatible with ROM change

Power control board is compatible with PAL change and two added wires if reset functions are desired - RECOMMENDED

Host interface boards are compatible with reduced image transfer speed, about a factor of 2. Different PALs required in timing board- ??

Controller housing, power supply fully compatible

New timing, video processor and clock driver boards required - old analog boards will NOT work with new timing board, and vice versa.

Power Distribution

+/- 16V from PS regulated to +/- 15V, +/- 5V on video board,
+/- 12V on clock driver

+5V not regulated anywhere

Cable drops the voltage so user should check it on controller boards, esp. 5V

OnCE Port in-circuit emulator for DSP debug on timing board

-> How to purchase

DSP software toold - Motorola assembler

-> How to purchase