



# TECHNICAL MEMORANDUM

Title: Correcting errors induced by incomplete detector output settling		TM: STScI-NGST-TM-2002- Date: 0003A Rev.: 4 March 2002
Authors: <i>D. Figer, B. J. Rauscher, M. Regan, G. A. Kriss, &amp; S. Balleza</i>	Phone: (410)338-4377	Approvals: Peter Stockman

## 1. Introduction

The purpose of this memo is to determine how accurately one can correct detector output signals for incomplete settling as a function of settling time, uncertainty in settling time, and sampling time.

## 2. Analytical Model of Detector Output Response

A detector's output voltage is dependent on the amount of charge on the pixel to which it is connected. This voltage will change as the output is connected to pixels with differing charge levels. The output voltage will settle to the asymptotic value in an amount of time that depends on characteristics of the detector output electronics, the output cable, and downstream analog electronics. We can partially correct a read of an incompletely settled voltage level by assuming a characteristic settling curve.

If we assume that the settling is perfectly fit by an exponential, we find that the output voltage is given by:

$$V_i(t) = V_i(\infty) - (V_i(\infty) - V_{i-1}(\tau)) \exp^{-t/t_{\text{settle}}}$$

where  $i$  is the pixel being read,  $\tau$  is the sample time, and  $t_{\text{settle}}$  is the settling time. Using this equation, we could predict  $V_i(\infty)$  by measuring the unsettled voltage,  $V_i(\tau)$ , and comparing it to the voltage level of the output for the previous pixel,  $V_{i-1}(\tau)$ . So,

$$V_{i,\text{predicted}}(\infty) = \frac{V_{i,\text{noisy}}(\tau) - V_{i-1,\text{noisy}}(\tau) \exp^{-\tau/t_{\text{settle}}}}{1 - \exp^{-\tau/t_{\text{settle}}}}$$

where "noisy" means that the voltages include whatever read noise exists.

The error in this predicted value is

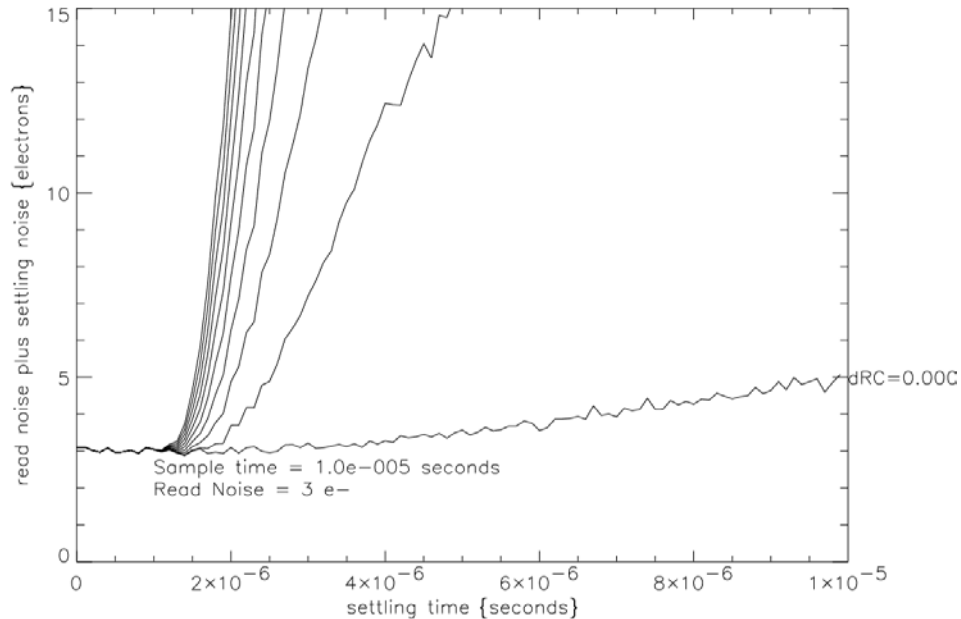
$$error = V_{i,predicted} - V_i(\infty) = \frac{n_{r,i-1} \exp^{-\tau/t_{settle}} - n_{r,i}}{1 - \exp^{-\tau/t_{settle}}}$$

where  $n_{r,i-1}$  and  $n_{r,i}$  represent the small deviations from true values due to read noise. Note that in the case where  $\tau/t_{settle}$  approaches infinity, the signal is fully settled, and the error approaches the read noise. However, if  $\tau/t_{settle}$  is comparable to 1, then the effective error in our approximation is significantly in excess of the read noise.

### 3. Simulation of Settling Time Noise

There is an additional error if our knowledge of  $t_{settle}$  is not perfect. To simulate what effect this would have on the error, we wrote a program that estimates the error from the equations above for a range of uncertainties in  $t_{settle}$ . We assumed that the true pixel values are  $0 e^-$  and  $5000 e^-$ . These values represent a pixel exposed to very little flux and a pixel hit by a cosmic ray, a combination that might be relevant for the NIRSPEC. The read noise and the error in the settling time were both modeled by a Gaussian distribution.

Figure 1 shows the read noise plus approximation noise (settling noise) for a range of settling times and uncertainties in the settling times. The case for  $n_r=3 e^-$  is presented. The settling time is on the x-axis and is called the RC time constant. The standard deviation in settling time error is “dRC”. This simulation shows that RC must be small or the errors become prohibitive.

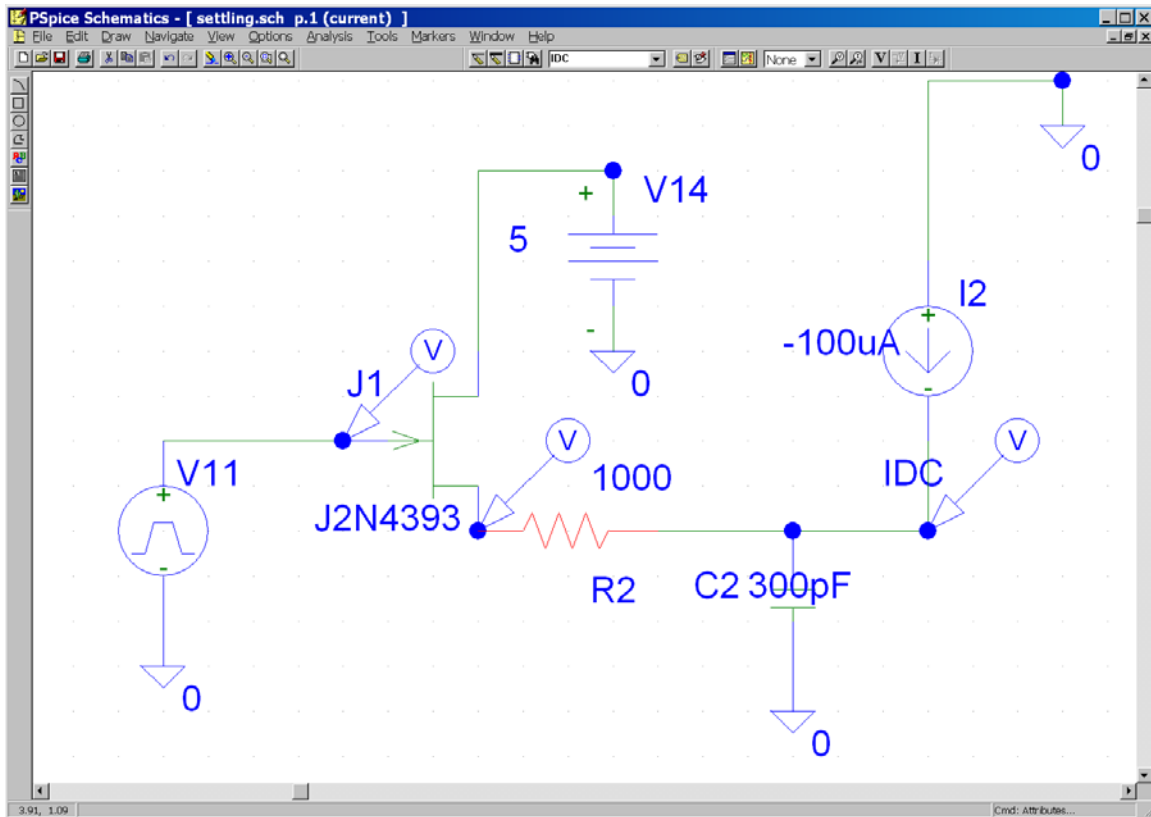


**Figure 1. Read noise plus approximation noise versus settling time for a range of uncertainty in knowledge about settling time. The uncertainty in settling time is incremented by 1% for each curve, starting with zero uncertainty (dRC=0.000).**

#### 4. Limitations and Transimpedance of the Output FET

So far, we have assumed that the detector output is perfectly described by an exponential. In reality, we know that the transimpedance of the output FET changes as a function of signal swing, so clearly the settling time is not constant for all pixel values and the output impedance actually changes during settling. This effect was modeled using the SPICE circuit in Figure 2.

We used the J2N43943 (J1) to represent the detector output FET. Note that this part is not meant to represent an exact copy of what might be found in a detector. We modeled the output cable as an RC circuit (R2 and C2). The output is sourced by an ideal current source providing 100  $\mu\text{A}$  of current. The pixel response is modeled as a step function (V11), with a delay of 500 ns.



**Figure 2. SPICE model of detector output, with cable represented as an RC circuit and current source.**

Figure 3a shows the input and output voltages for this circuit as functions of time. The input pulse is a sharp step function at  $t=500$  ns. The response at the FET source has an exponential rise. The response at the end of the cable is rather slow as a result of the output impedance and capacitance. Figure 3b shows the FET transimpedance as a function of time. Note that the transimpedance is a strong function of time. This suggests that one cannot easily know the “R” in the analysis described in this memo.

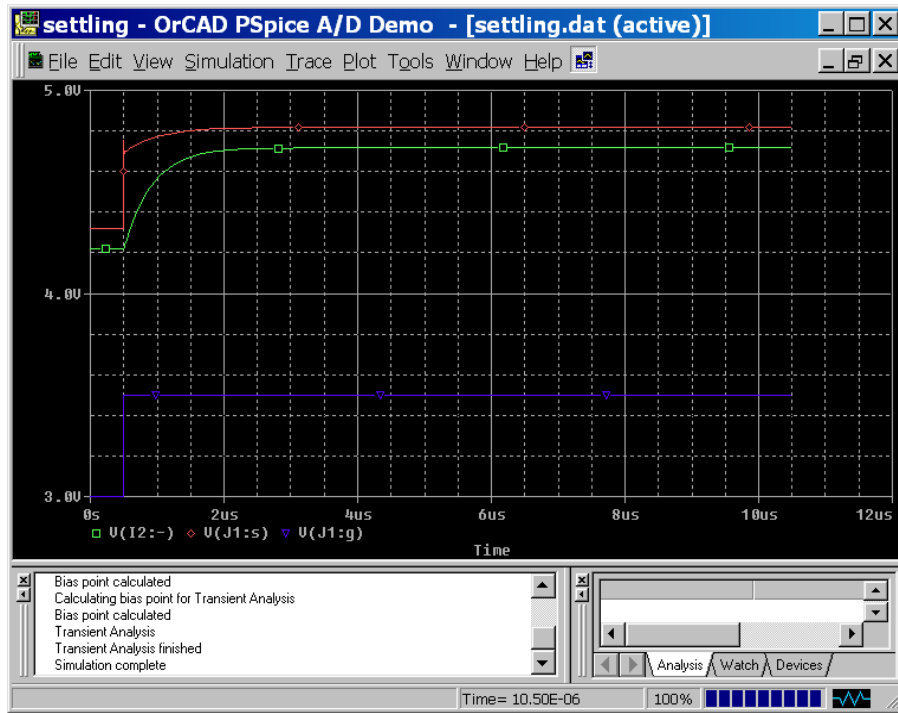


Figure 3a. Response to input pulse at FET output and end of cable.

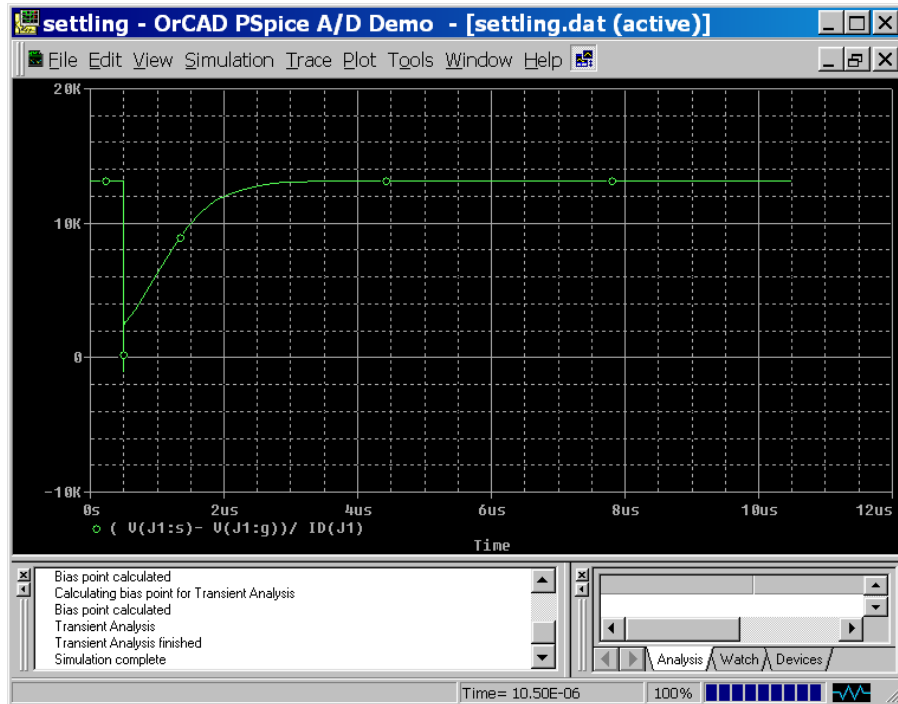


Figure 3b. Transimpedance for a step function input at the output FET gate.

## 5. Conclusions

The analysis in this memo suggests that little settling time noise will be incurred if the RC time constant of the output cable is kept to  $<1/10$  of the sampling time. Indeed, given that some output cables can deliver effective output RCs of less than 250 ns, we recommend that the NGST cables be specified to deliver this level of performance, or better. Faster settling times offer the possibility of sampling times less than 10  $\mu$ s and associated benefits in reducing noise by employing averaging techniques. We also recommend that an engineering study be done to simulate the effects of a varying system impedance as a function of time due to the dynamic nature of the transimpedance of the output FET, as well as other sources.

## 6. Products

This document, the IDL code used to produce it, the SPICE model, and the plots can be found at:

<http://idtl.stsci.edu/products/settling%20time/>